Madenat Alelem University College

Medical Physics Department

كلية مدينة العلم الجامعة

قسم الفيزياء الطبية

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Assist. Lect.

Shahad A. Al-Saqal

Semiconductor Basics

Conductor, Insulator and Semiconductor

Conductors

A conductor is a material that easily conducts electrical current. The best conductors are single-element materials, such as copper, silver, gold, and aluminum, which are characterized by atoms with only one valence electron very loosely bound to the atom. These loosely bound valence electrons can easily break away from their atoms and become free electrons. Therefore, a conductive material has many free electrons that, when moving in the same direction, make up the current.

Insulators

An insulator is a material that does not conduct electrical current under normal conditions. Most good insulators are compounds rather than single-element materials. Valence electrons are tightly bound to the atoms; therefore, there are very few free electrons in an insulator.

Semiconductors

A semiconductor is a material that is between conductors and insulators in its ability to conduct electrical current. A semiconductor in its pure (intrinsic) state is neither a good conductor nor a good insulator. The most common single-element semiconductors are silicon, germanium, and carbon. Compound semiconductors such as gallium arsenide are also commonly used. The single-element semiconductors are characterized by atoms with four valence electrons.

Energy Bands

The valence shell of an atom represents a band of energy levels and that the valence electrons are confined to that band. When an electron acquires enough additional energy, it can leave the valence shell, become a free electron, and exist in what is known as the **conduction band**.

The difference in energy between the valence band and the conduction band is called an energy gap. This is the amount of energy that a valence electron must

have in order to jump from the valence band to the conduction band. Once in the conduction band, the electron is free to move throughout the material and is not tied to any given atom.

Figure (1) shows energy diagrams for insulators, semiconductors, and conductors. Notice in part (A) that insulators have a very wide energy gap. Valence electrons do not jump into the conduction band except under breakdown conditions where extremely high voltages are applied across the material. As you can see in part (B), semiconductors have a much narrower energy gap. This gap permits some valence electrons to jump into the conduction band and become free electrons. By contrast, as part (C) illustrates, the energy bands in conductors are overlap. In a conductive material there is always a large number of free electrons.

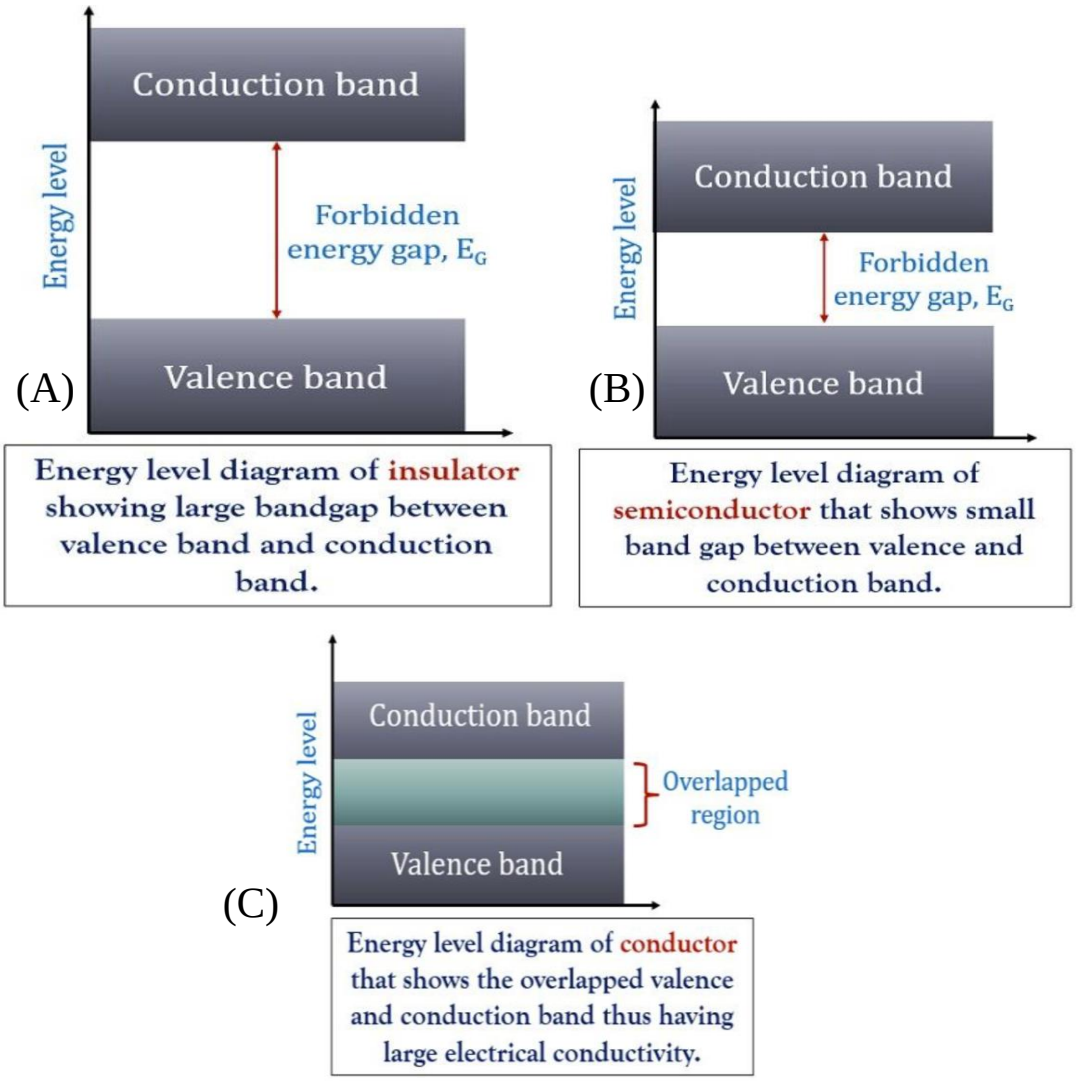


Figure (1): The energy level diagram of A) insulator, B) semiconductor, C) conductor

Types of Semiconductors:

I. Intrinsic (Pure) Semiconductors

An intrinsic semiconductor is one which is made of the semiconductor material in its pure form, such as pure germanium and pure silicon which have forbidden energy gaps of 0.72 eV and 1.1 eV respectively. The energy gap is so small that even at ordinary room temperature; there are many electrons which possess sufficient energy to jump across the small energy gap between the valence and the conduction bands.

Alternatively, an intrinsic semiconductor may be defined as one in which the number of conduction electrons is equal to the number of holes.

The atomic structures of pure silicon and pure germanium are shown in Figure (2). Silicon is the most widely used material in diodes, transistors, integrated circuits, and other semiconductor devices. Notice that both silicon and germanium have the same four valence electrons.

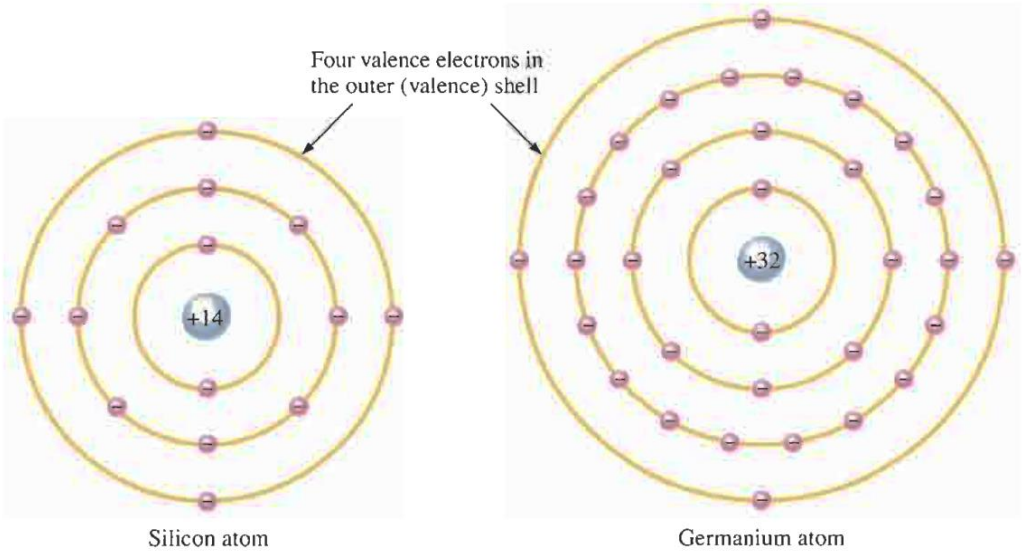


Figure (2): The Silicon and Germanium atoms

The valence electrons in germanium are in the fourth shell while those in silicon are in the third shell, closer to the nucleus. This means that the germanium valence electrons are at higher energy levels than those in silicon and, therefore, require a smaller amount of additional energy to escape from the atom. This property makes germanium more unstable at high temperatures, and this is a basic reason why silicon is the most widely used semi-conductive material.

II. Extrinsic Semiconductors

Semiconductor materials do not conduct current well and are of limited value in their intrinsic state. This is because of the limited number of free electrons in the conduction band and holes in the valence band. Intrinsic silicon (or germanium) must be modified by increasing the number of free electrons or holes to increase its conductivity and make it useful in electronic devices. This is done by adding impurities to the intrinsic material, this process is called ***Doping***. Two types of extrinsic semiconductor materials, n-type and p-type.

N-Type Semiconductor

To increase the number of conduction-band electrons in intrinsic silicon, pentavalent impurity atoms are added. These are atoms with five valence electrons such as arsenic (As), phosphorus (P), bismuth (Bi), and antimony (Sb).

Figure (3) shows (A) the pure silicon crystal and (B) pentavalent atom (e.g., antimony) forms covalent bonds with four adjacent silicon atoms. Four of the antimony atom's valence electrons are used to form the covalent bonds with silicon atoms, leaving one extra electron. This extra electron becomes a conduction electron because it is not attached to any atom. Because the pentavalent atom gives up an electron, it is often called a donor atom. The number of conduction electrons can be carefully controlled by the number of impurity atoms added to the silicon. A conduction electron created by this doping process does not leave a hole in the valence band because it is in excess of the number required to fill the valence band.

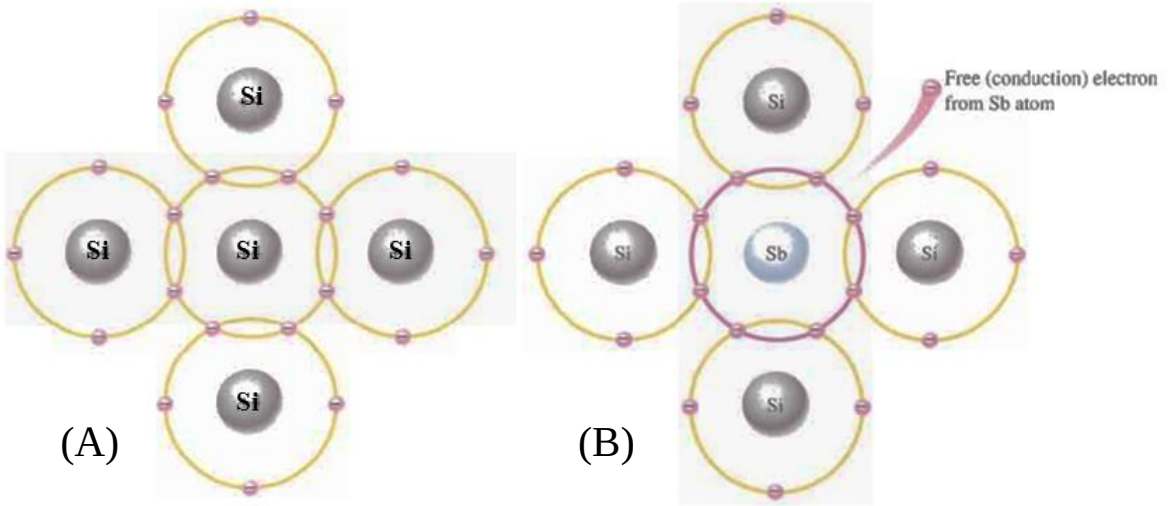


Figure (3): A) Pure Silicon, B) Impurity Silicon crystals

P-Type Semiconductor

To increase the number of holes in intrinsic silicon, trivalent impurity atoms are added. These are atoms with three valence electrons such as boron (B), indium (In), and gallium (Ga).

As shown in Figure (4), each trivalent atom (e.g., boron) forms covalent bonds with four adjacent silicon atoms. All three of the boron atom's valence electrons are used in the covalent bonds; and, since four electrons are required, a hole results when each trivalent atom is added. Because the trivalent atom can take an electron, it is often referred to as an acceptor atom. The number of holes can be carefully controlled by the number of trivalent impurity atoms added to the silicon. A hole created by this doping process is not accompanied by a conduction (free) electron.

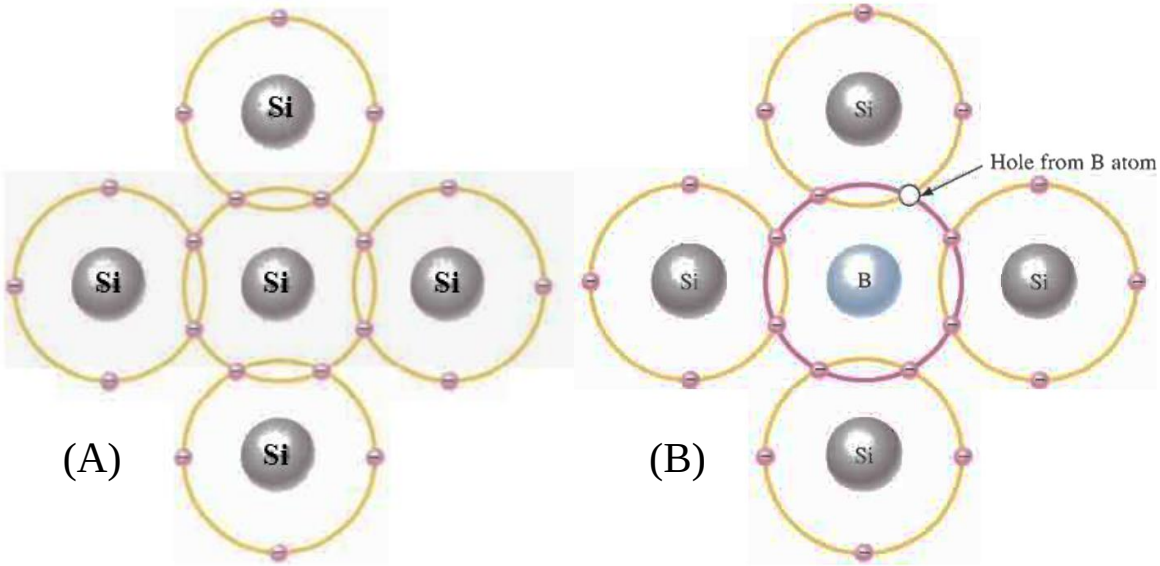


Figure (4): A) Pure Silicon, B) Impurity Silicon crystals

Majority and Minority Carriers

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence band that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes has not changed significantly from this intrinsic level. The net result,

therefore, is that the number of electrons far outweighs the number of holes. For this reason:

In n-type material (Figure 5a) the electron is called the majority carrier and the hole the minority carrier.

For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Figure (5b). Therefore:

In p-type material the hole is the majority carrier and the electron is the minority carrier.

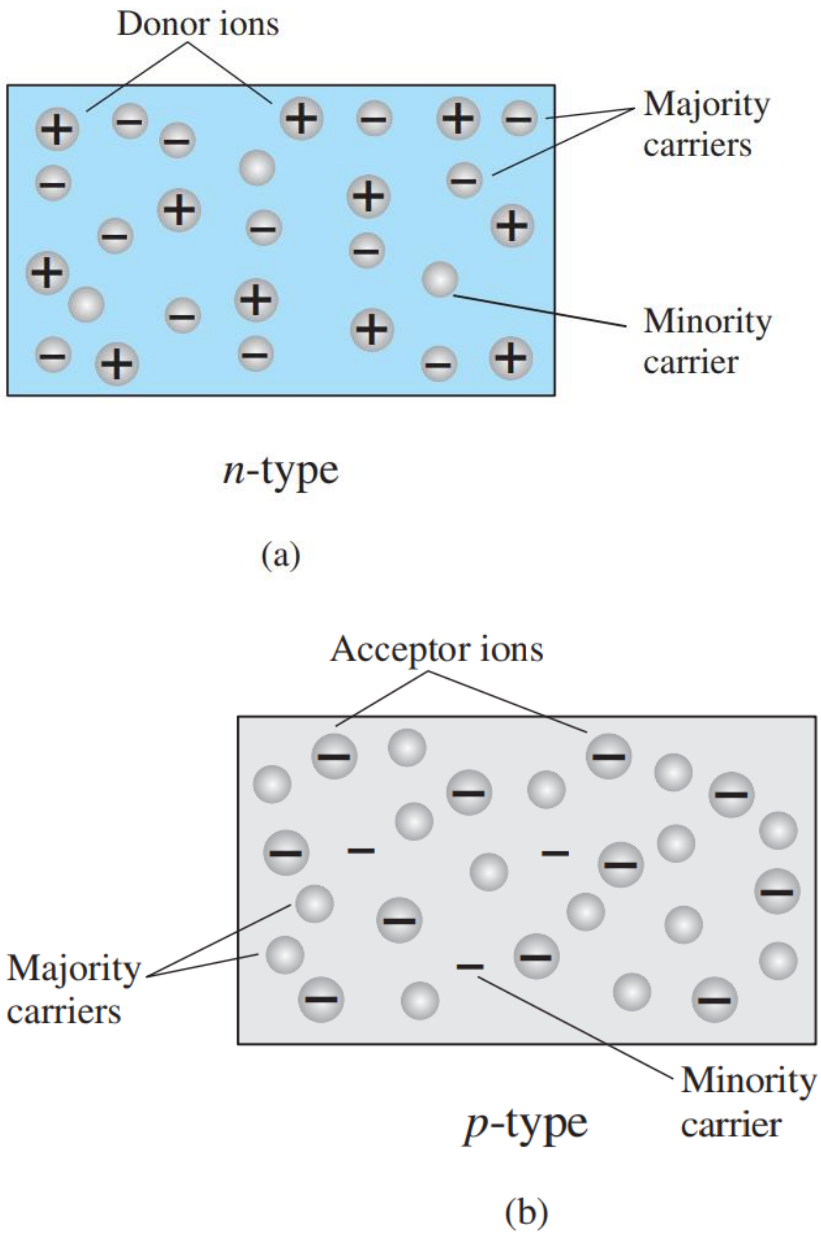


Figure (5): (a) n-type material; (b) p-type material.

The Semiconductor Diode (PN Junction)

Introduction

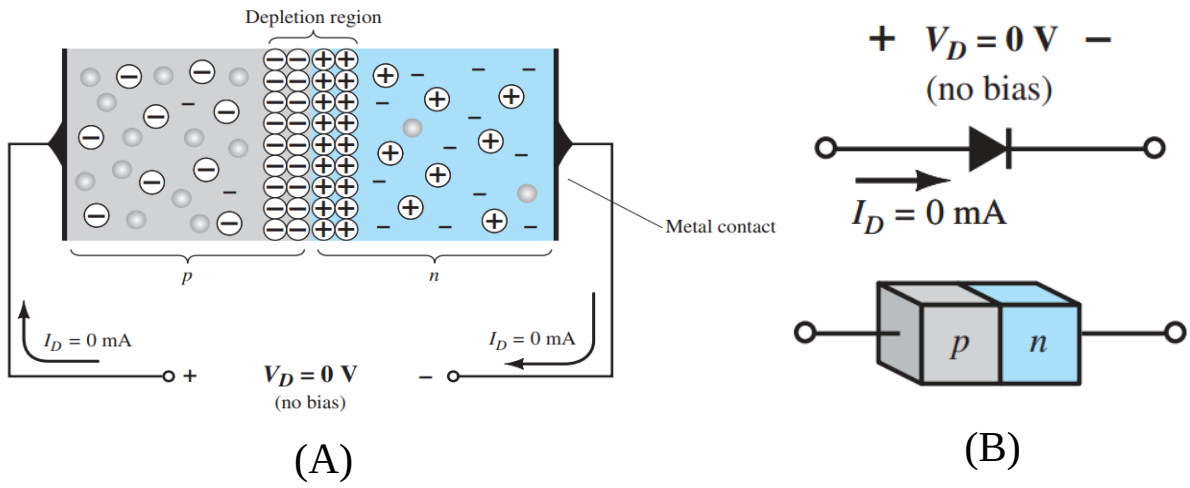
Now that both n- type and p-type materials are available, we can construct our first solid-state electronic device: **The semiconductor diode**, is created by simply joining n-type and p-type material together, nothing more, just the joining of one material with a majority carrier of electrons to one with a majority carrier of holes.

The n-type and p-type materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Figure (6A). Note in Figure (6A) that the only particles displayed in this region are the positive and the negative ions remaining once the free carriers have been absorbed.

This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.

In Figures (6A & 6B) there is no-bias because there is no external voltage applied. In Figure (6B) the symbol for a semiconductor diode is provided to show its correspondence with the *p–n* junction. In each figure it is clear that the applied voltage is 0 V (no bias) and the resulting current is 0 A, much like an isolated resistor. The absence of a voltage across a resistor results in zero current through it. Even at this early point in the discussion it is important to note the polarity of the voltage across the diode in Figure (6B) and the direction given to the current. Those polarities will be recognized as the *defined polarities* for the semiconductor diode.

Under no-bias conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region for any reason will pass quickly into the *p*-type material. The closer the minority carrier is to the junction, the greater is the attraction for the layer of negative ions and the less is the opposition offered by the positive ions in the depletion region of the *n*-type material. We will conclude, therefore, that any minority carriers of the *n*-type material that find themselves in the depletion region will pass directly into the *p*-type material.



(A) (B)

Figure (6): A p–n junction with no external bias: (A) an internal distribution of charge; (B) a diode symbol, with the defined polarity and the current direction

The majority carriers (electrons) of the n-type material must overcome the attractive forces of the layer of positive ions in the n-type material and the shield of negative ions in the p-type material to migrate into the area beyond the depletion region of the p-type material. However, the number of majority carriers is so large in the n-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the p-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the p-type material.

In summary, therefore: *In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.*

In other words, the current under no-bias conditions is zero, as shown in Figures (6A&B).

Diode biasing

I. *Reverse biasing*

If an external potential of V volts is applied across the p–n junction such that the positive terminal is connected to the n-type material and the negative terminal is connected to the p-type material as shown in Figure (7), the number of uncovered positive ions in the depletion region of the n-type material will increase due to the large number of free electrons drawn to the positive potential of the applied

voltage. For similar reasons, the number of uncovered negative ions will increase in the p-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero, as shown in Figure (7a).

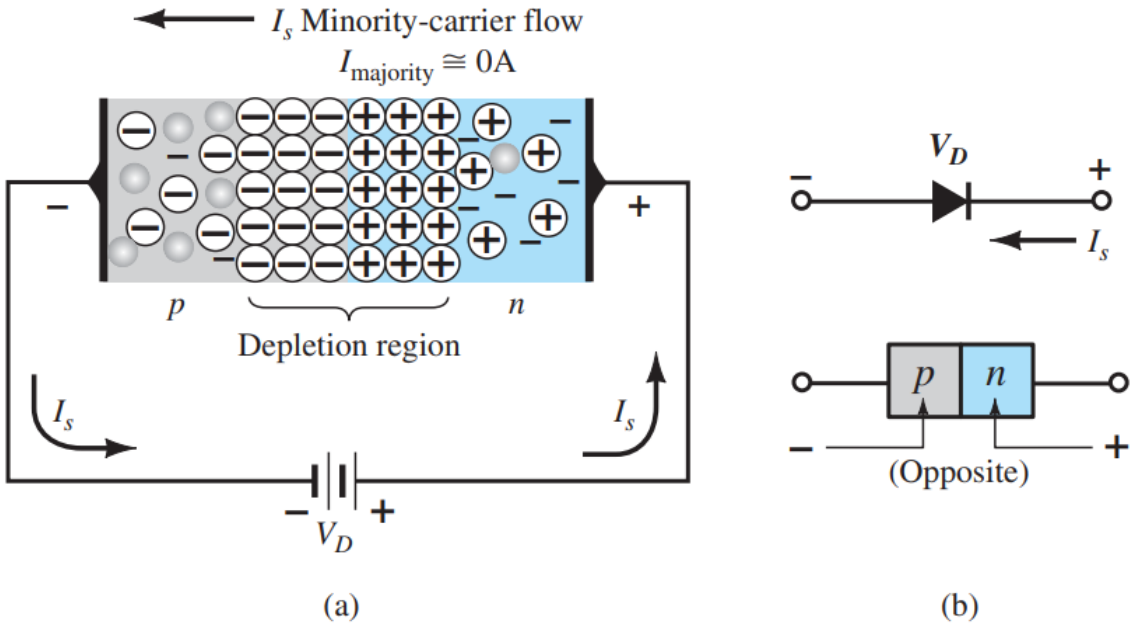


Figure (7): Reverse-biased p–n junction: (a) internal distribution of charge under reverse-bias conditions; (b) reverse-bias polarity and direction of reverse saturation current.

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s.

The reverse saturation current is seldom more than a few microamperes and typically in nA, except for high-power devices. The term saturation comes from the fact that it reaches its maximum level quickly and does not change significantly with increases in the reverse-bias potential, as shown on the diode characteristics of Figure (9) for $V_D < 0V$. The reverse-biased conditions are depicted in Figure (7b) for the diode symbol and p–n junction. Note, in particular, that the direction of it's against the arrow of the symbol. Note also that the negative side of the applied voltage is connected to the p-type material and the positive side to the n-type material, the difference in underlined letters for each region revealing a reverse-bias condition.

II. *Forward biasing*

A forward-bias or "on" condition is established by applying the positive potential to the p-type material and the negative potential to the n-type material as shown in Figure (8). The application of a forward-bias potential VD will "pressure" electrons in the n-type material and holes in the p-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Figure (8a). The resulting minority-carrier flow of electrons from the p-type material to the n-type material (and of holes from the n-type material to the p-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the n-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p-type material. As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. (9). Note that the vertical scale of Figure (9) is measured in milli-amperes (although some semiconductor diodes have a vertical scale measured in amperes), and the horizontal scale in the forward-bias region has a maximum of 1 V. Typically, therefore, the voltage across a forward-biased diode will be less than 1 V. Note also how quickly the current rises beyond the knee of the curve.

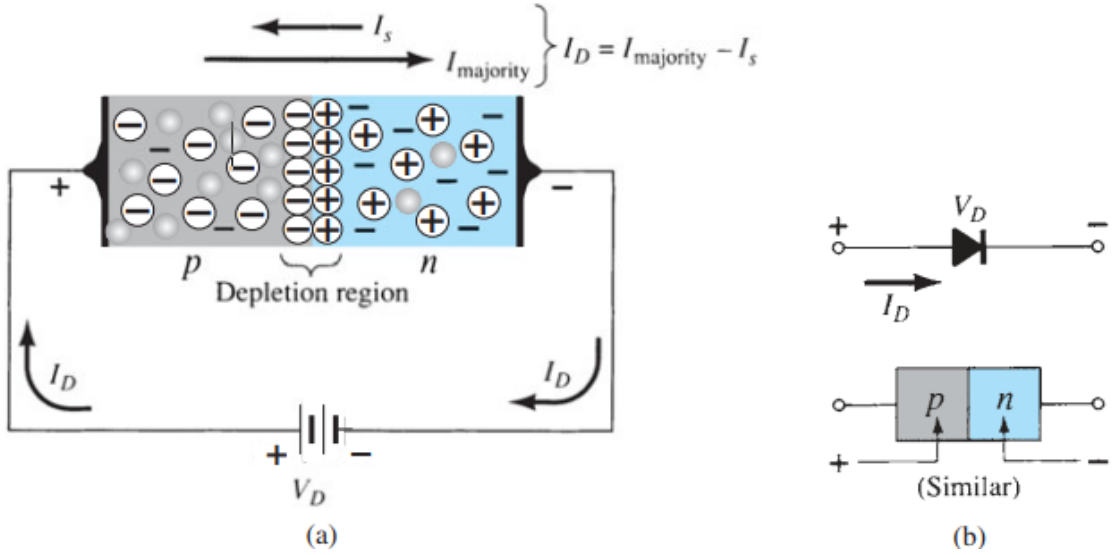


Figure (8): Forward-biased p–n junction: (a) internal distribution of charge under forward-bias conditions; (b) forward-bias polarity and direction of resulting current

Diode Characteristics

Figure (9) shows the static voltage current characteristics for a low power P-N junction diode.

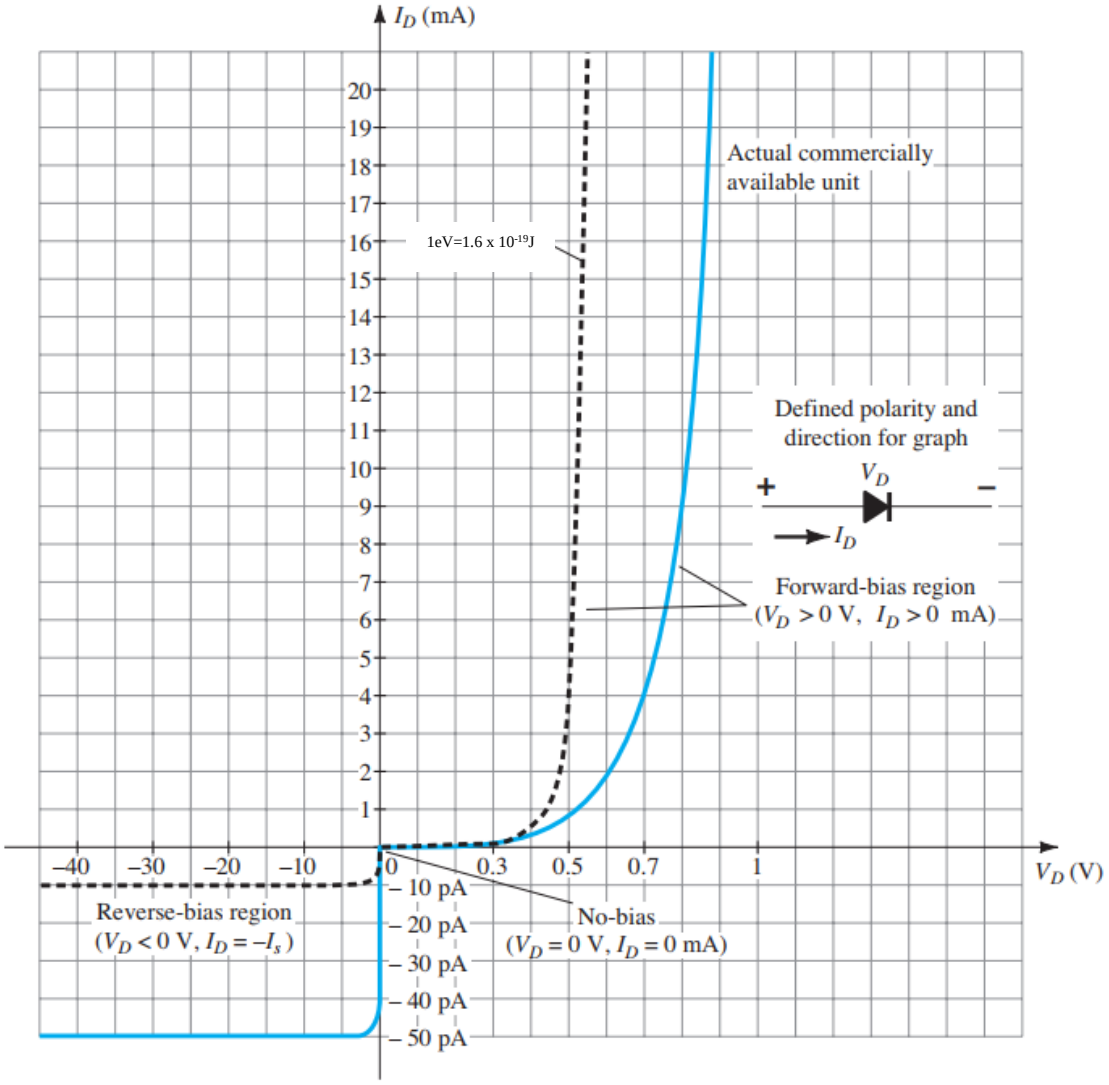


Figure (9): Diode Characteristic

Forward characteristic

When the diode is forward biased and applied voltage is increased from zero hardly any current flows through the device in the beginning. It is because the external voltage is being opposed by the internal barrier voltage V_B whose value is 0.7 V for Si and 0.3 V for Ge as shown in figure (10). As soon as V_B is neutralized, current through the diode increases rapidly with increasing applied battery voltage. It is found that as little a voltage as 1.0 V produces a forward current of about 50 mA.

Reverse characteristic

When the diode is reverse biased majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. As the reverse voltage is increased from zero, there is a point where the application of too negative a voltage with the reverse polarity will result in a sharp change in the characteristics, as shown in Figure (10). The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the ***breakdown potential*** and is given the label V_{BV}. It is of order of pico-amperes (pA) for Si and micro-amperes (µA) for Ge. As seen from figure (10) when reverse voltage V_{BV}, the leakage current suddenly and sharply increases, the curve indicating zero resistance at this point.

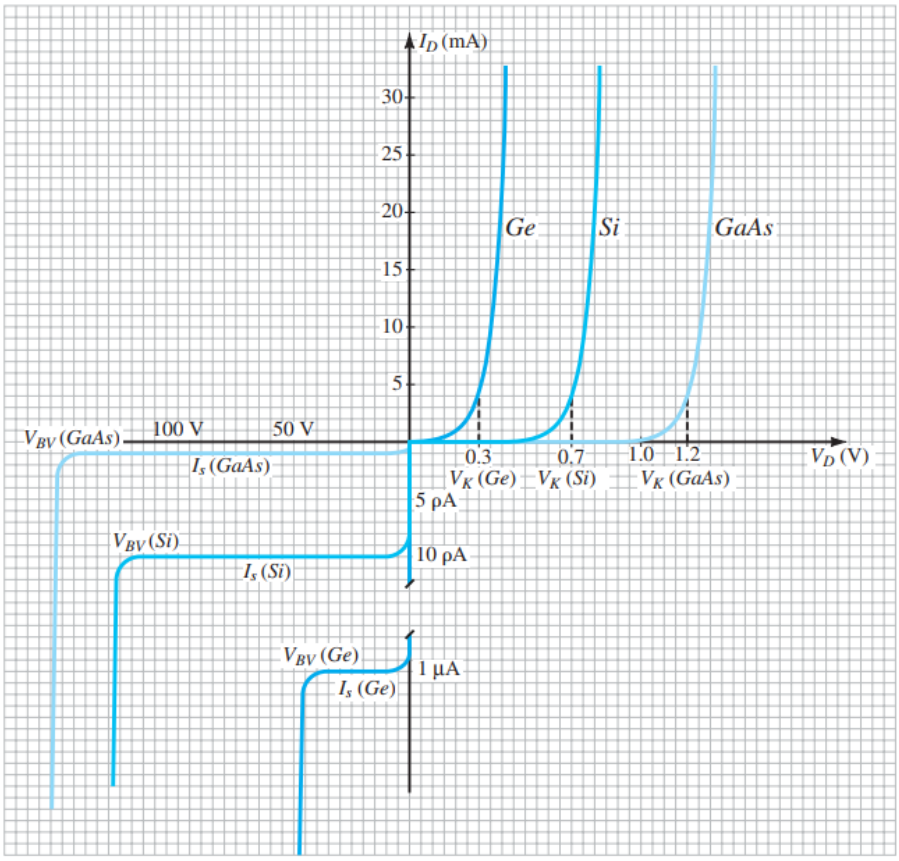


Figure (10): Comparison of Ge,Si, and GaAs commercial diodes

The breakdown region of the semiconductor diode described must be avoided if the response of a system is not to be completely altered by the sharp change in characteristics in this reverse-voltage region.

The maximum reverse-bias potential that can be applied before entering the breakdown region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted the P_{RV} rating).

If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.

Zener Diode

Introduction:

Zener diode is a silicon pn junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of a zener diode is set by carefully controlling the doping level during manufacture. If a zener diode is forward-biased, it operates the same as a rectifier diode.

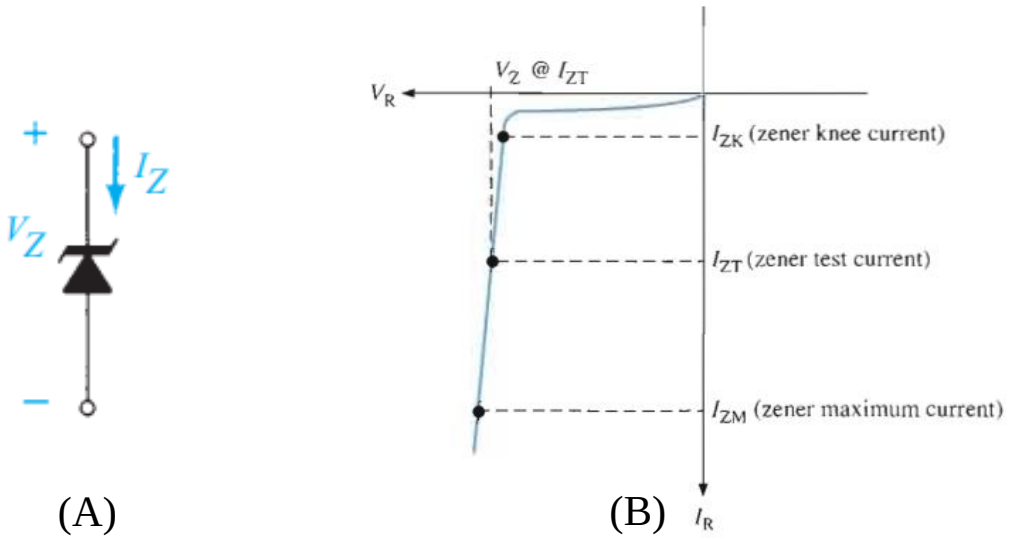
Zener breakdown

Zener breakdown occurs in a zener diode at low reverse voltages. A zener diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (Vz), the field is intense enough to pull electrons from their valence bands and create current.

Zeners are commercially available with breakdown voltages of 1.8V to 200V with specified tolerances from 1% to 20%.

Breakdown Characteristics

Figure (11) shows the reverse portion of a zener diode's characteristic curve. Notice that as the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the zener break down voltage (V_Z) remains essentially constant although it increases slightly as the zener current,I_Z, increases.



(A) (B)

Figure (11): A) The symbol, and B) The reverse characteristic of a zener diode

Zener Regulation

The ability to keep the reverse voltage across its terminals essentially constant is the key feature of the zener diode. A zener diode operating in breakdown acts as a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse-current values.

A minimum value of reverse current, I_{ZK}, must be maintained in order to keep the diode in breakdown for voltage regulation. You can see on the curve in Figure (11) that when the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also, there is a maximum current, I_{ZM}, above which the diode may be damaged due to excessive power dissipation. So, basically, the zener diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from I_{ZK} to I_{ZM}. A nominal zener voltage, V_{ZT}, is usually specified on a data sheet at a value of reverse current called the zener test current, I_{ZT}.

Diode Applications

The applications of diode are:

1. Rectifier circuits
   I. Half-wave rectifier
   II. Full-wave rectifier
2. Clipper circuits
3. Clamper circuits

Rectifier Circuits

The rectifier converts the AC input voltage to a pulsating DC voltage. The rectifier can be either a half-wave rectifier or a full-wave rectifier.

I. Half-wave rectifier

Figure (12) illustrates the process called half-wave rectification. A diode is connected to an AC source and to a load resistor, R, forming a half-wave rectifier. Keep in mind that all ground symbols represent the same point electrically. Let's examine what happens during one cycle of the input voltage using the ideal model for the diode. When the sinusoidal input voltage (Vi) goes positive, the diode is forward-biased and conducts current through the load resistor, as shown in Figure (12-a). The current produces an output voltage across the load R, which has the same shape as the positive half-cycle of the input voltage.

When the input voltage goes negative during the second half of its cycle, the diode is reverse-biased. There is no current, so the voltage across the load resistor is 0V, as shown in Figure (12-b). The net result is that only the positive half-cycles of the AC input voltage appear across the load. Since the output does not change polarity, it is a pulsating DC voltage with a frequency of 1/T Hz, as shown in Figure (12-c).

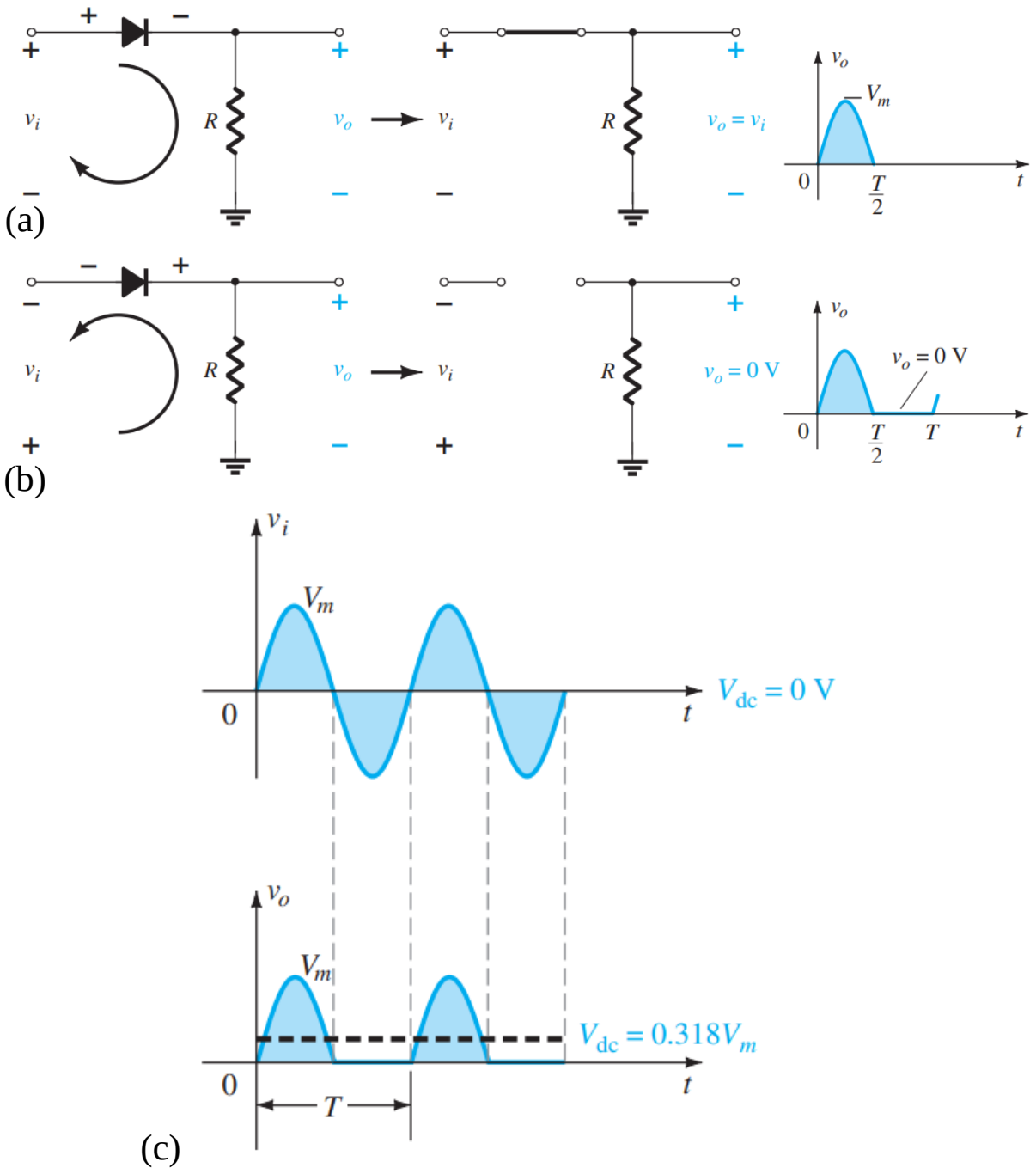
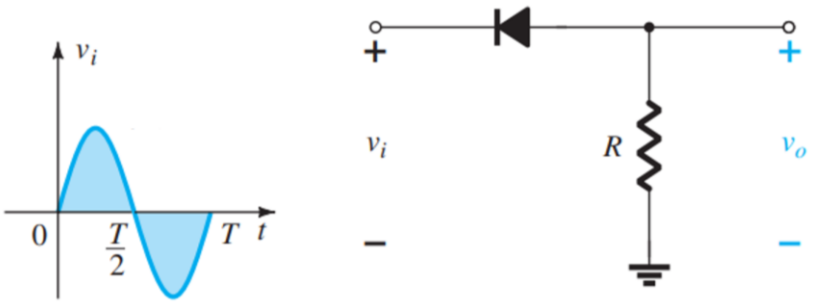


Figure (12): Half-wave rectifier operation

Homework: Sketch how does the diode act in this circuit, then sketch the Vo.

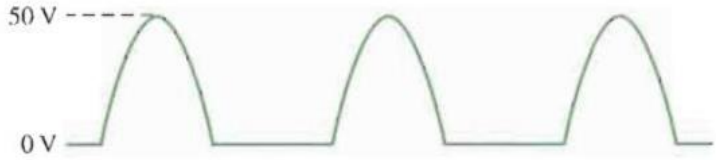


Average Value of the Half-Wave Output Voltage

The average value of the half-wave rectified output voltage is the value you would measure on a DC voltmeter. Mathematically, it is determined by finding the area under the curve over a full cycle, and then dividing by π, the number of radians in a half cycle. The result of this is expressed in Equation 1, where Vp or Vm is the peak (maximum) value of the voltage. This equation shows that V_{AVG} is approximately 31.8% of Vp for a half-wave rectified voltage.

$$V_{AVG} = \frac{V_p}{\pi} \; or \; V_{AVG} = 0.318 * V_p$$

Example 1: What is the average value of the half-wave rectified voltage in the next Figure?



Or: Determine the average value of the half-wave voltage if its peak (or maximum) amplitude is 50V.

Solution:

$$V_{AVG} = \frac{V_p}{\pi}$$

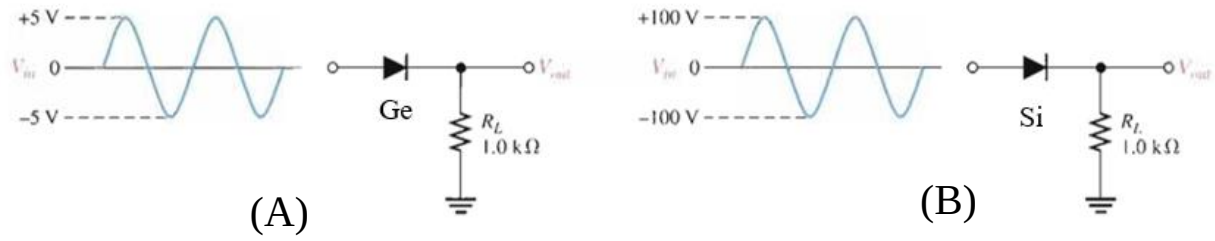
$$V_{AVG} = \frac{50}{3.14} = 15.9V$$

Effect of the Barrier Potential on the Half-Wave Rectifier Output

In the previous discussion, the diode was considered ideal. When the practical diode model is used with the barrier potential of V_k taken into account, this is what happens. During the positive half-cycle, the input voltage must overcome the barrier potential before the diode becomes forward-biased. This results in a half-wave output with a peak value that is V_k less than the peak value of the input. If the diode was silicon, V_k=0 but if the diode was Ge, V_k=0.3V. The expression for the peak output voltage is

$$V_{p(out)} = V_{p(in)} - V_k$$

Example 2: Determine the output voltages of each rectifier for the indicated input voltages, as shown in the next Figure.



The peak output voltage for circuit (A) is

$$V_{p(out)} = V_{p(in)} - V_k$$

$$V_{p(out)} = 5 - 0.3 = 4.7V$$

The peak output voltage for circuit (B) is

$$V_{p(out)} = V_{p(in)} - V_k$$

$$V_{p(out)} = 100 - 0.7 = 99.3V$$

Note that, the effect of the barrier potential was neglected, when the peak value of the applied voltage is much greater than the barrier potential as shown in the circuit (B).

Peak Inverse Voltage (PIV)

The peak inverse voltage (PIV) equals the peak value of the input voltage, and the diode must be capable of withstanding this amount of repetitive reverse voltage. For the diode in Figure (13), the maximum value of reverse voltage, designated as PIV, occurs at the peak of each negative alternation of the input voltage when the diode is reverse-biased.

$$PIV = -V_{p(in)}$$

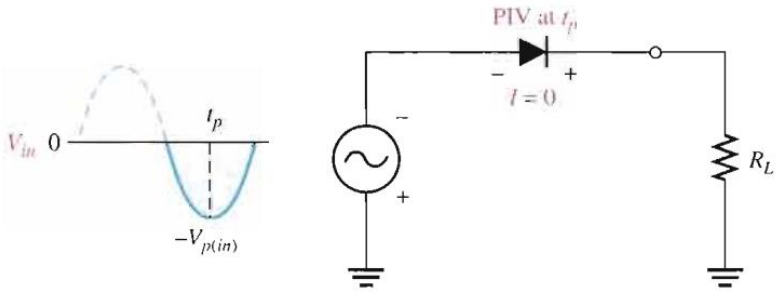
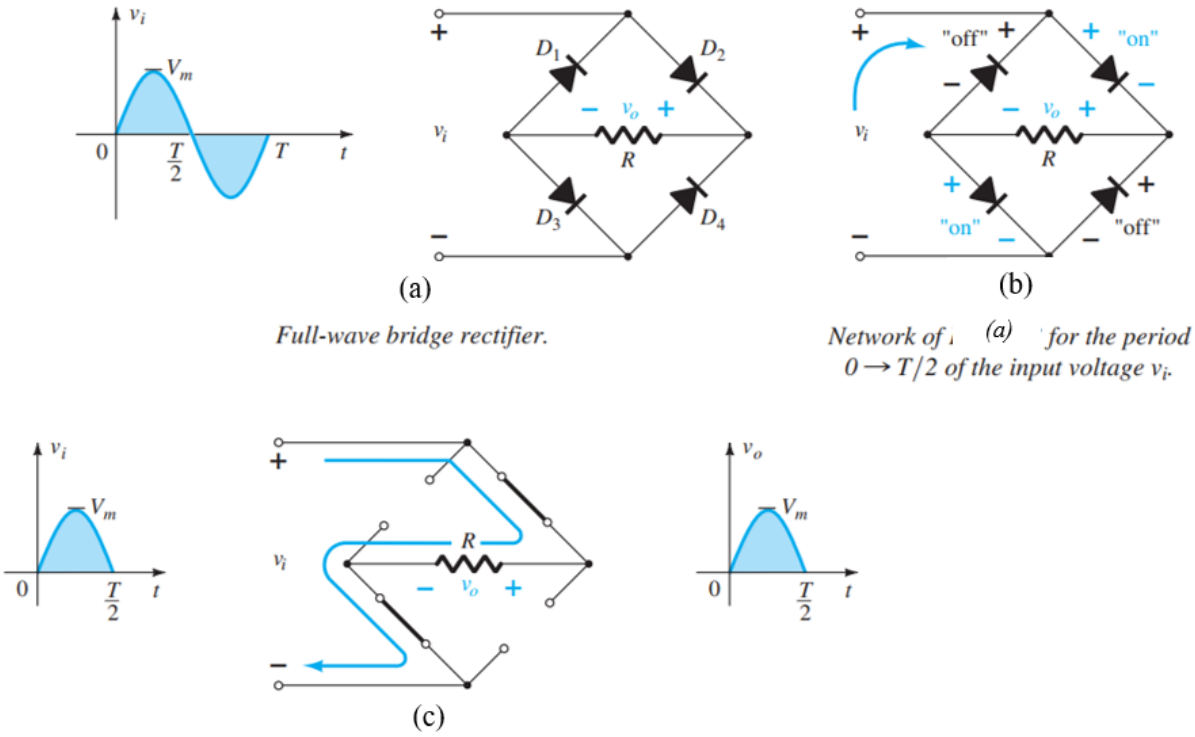


Figure (13): The PIV occurs at the peak of each half-cycle of the input

II. Full-wave rectifier

The DC level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Figure (14a) with its four diodes in a *bridge* configuration. During the period t 0 to T/2 the polarity of the input is as shown in Figure (14b). The resulting polarities across the ideal diodes are also shown in Fig. (14b) to reveal that D2 and D3 are conducting, where as D1 and D4 are in the "off" state. The net result is the configuration of Figure (14c), with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is Vo = Vi, as shown in the same figure.



Full-wave bridge rectifier.

Network of (a) for the period $0 \rightarrow T/2$ of the input voltage v_i.

Conduction path for the positive region of v_i.

Figure (14): Full-wave rectifier operation (first stage)

For the negative region of the input the conducting diodes are D1 and D4, resulting in the configuration of Figure (15). The important result is that the polarity across the load resistor R is the same as in Figure (14b), establishing a second positive pulse, as shown in Fig. (15). Over one full cycle the input and output voltages will appear as shown in Fig. (16).

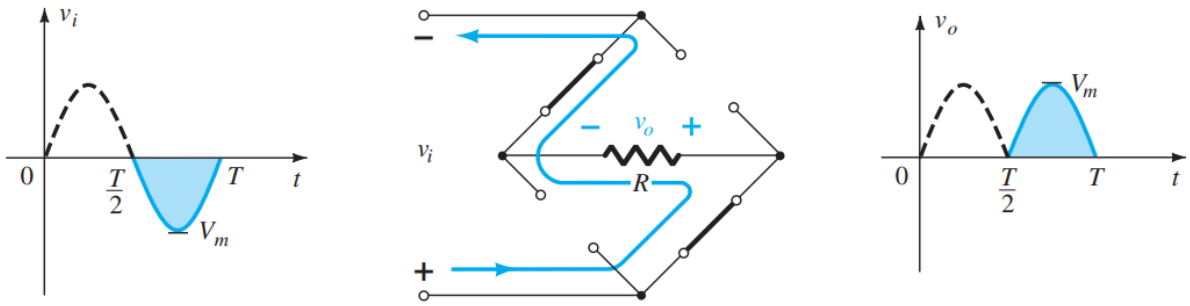


Figure (15): Full-wave rectifier operation (second stage)

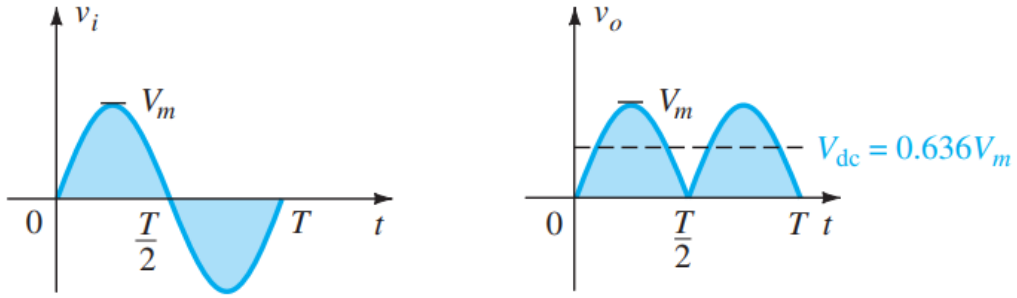


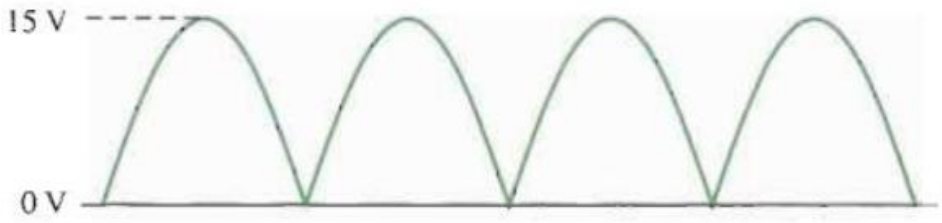
Figure (16): The input and output waveforms for a full-wave rectifier

Average Value of the Full-Wave Output Voltage

The number of positive alternations that make up the full-wave rectified voltage is twice that of the half-wave voltage for the same time interval. The average value, which is the value measured on a DC voltmeter, for a full-wave rectified sinusoidal voltage is twice that of the half-wave, as shown in the following formula:

$$V_{AVG} = \frac{2V_p}{\pi} \; or \; V_{AVG} = 0.636 * V_p$$

Example 3: Find the average value of the full-wave rectified voltage in the next Figure.



Solution:

$$V_{AVG} = \frac{2V_p}{\pi} = \frac{2 * 15}{3.14} = 9.55V$$

Effect of the Barrier Potential on the Full-Wave Rectifier Output

As you can see in Figures (14&15), two diodes are always in series with the load resistor during both the positive and negative half-cycles. If these diode drops are taken in to account, the output voltage is

$$V_{p(out)} = V_{p(in)} - 2V_k$$

Peak Inverse Voltage (PIV)

Let's assume that D1, and D2 are forward-biased and examine there-verse voltage across D3 and D4. Visualizing D1 and D2 as shorts (ideal model), you can see that D3 and D4 have a peak inverse voltage equal to the peak input voltage. Since the output voltage is ideally equal to the input voltage,

$$PIV = V_{p(out)}$$

Capacitor-Input Filter

Figure (17) illustrates the filtering concept showing a nearly smooth DC output voltage from the filter. The small amount of fluctuation in the filter output voltage is called ripple.

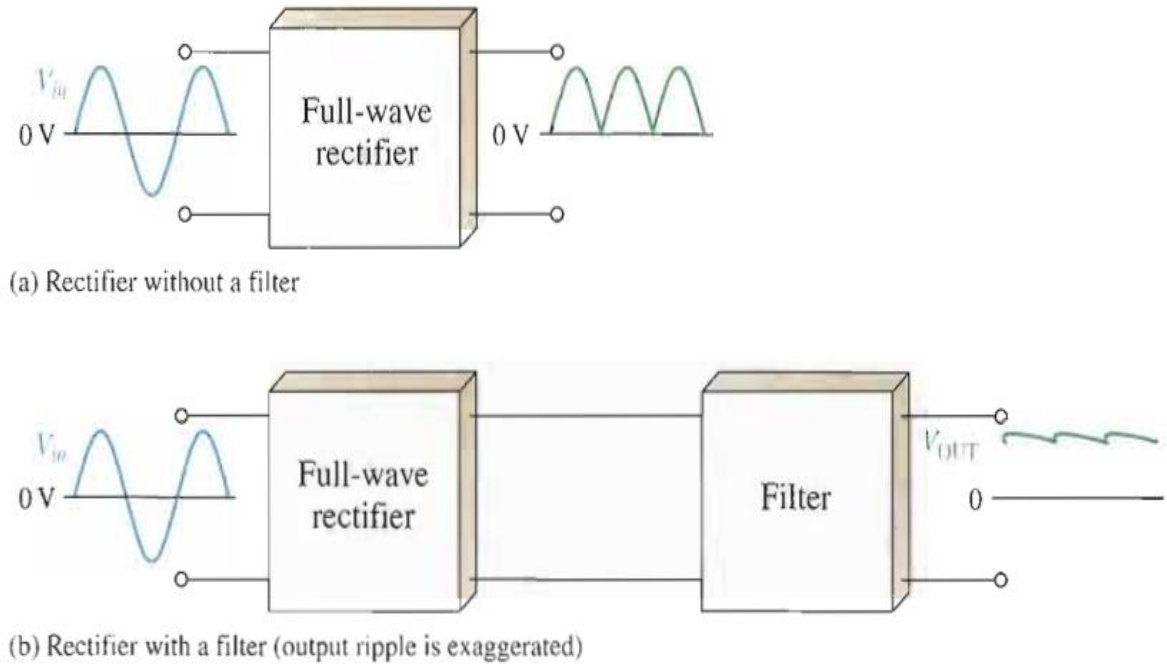


Figure (17): The filtering concept

A half-wave rectifier with a capacitor-input filter is shown in Figure (18). The filter is simply a capacitor connected from the rectifier output to ground. R_L represents the equivalent resistance of a load. We will use the half-wave rectifier to illustrate the basic principle and then expand the concept to full-wave rectification.

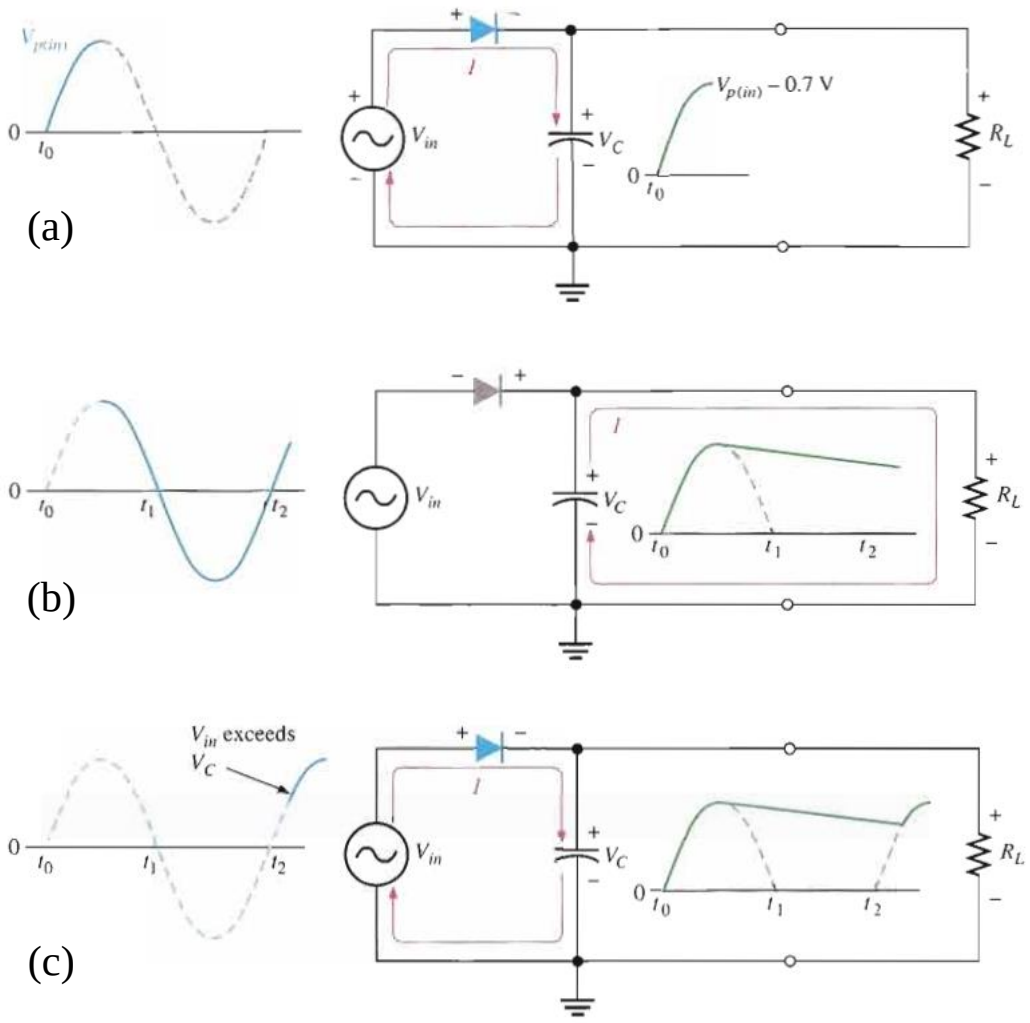


Figure (18): Half-wave rectifier with capacitor operation

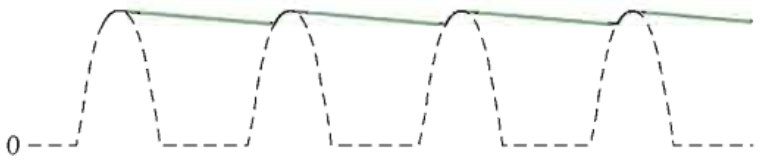
During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7V of the input peak, as illustrated in Figure (18-a). When the input begins to decrease below its peak, as shown in part (b), the capacitor retains its charge and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only through the load resistance at a rate determined by the RLC time constant, which is normally long compared to the

period of the input. The larger the time constant, the less the capacitor will discharge. During the first quarter of the next cycle, as illustrated in part (c), the diode will again be come forward-biased when the input voltage exceeds the capacitor voltage by approximately 0.7V.

Ripple Voltage

As you have seen, the capacitor quickly charges at the beginning of a cycle and slowly discharges through RL after the positive peak of the input voltage (when the diode is reverse-biased). The variation in the capacitor voltage due to the charging and discharging is called the ripple voltage. Generally, ripple is undesirable; thus, the smaller the ripple, the better the filtering action, as illustrated in Figure (19).

(a) Larger ripple means less effective filtering.



(b) Smaller ripple means more effective filtering. Generally, the larger the capacitor value, the smaller the ripple for the same input and load.

Figure (19): Half-wave ripple voltage waveform

For a full-wave rectifier (Figure 20) easier to filter because of the shorter time between peaks. When filtered, the full-wave rectified voltage has a smaller ripple than does a half-wave voltage for the same load resistance and capacitor values. The capacitor discharges less during the shorter interval between full-wave pulses, as shown in Figure (21).

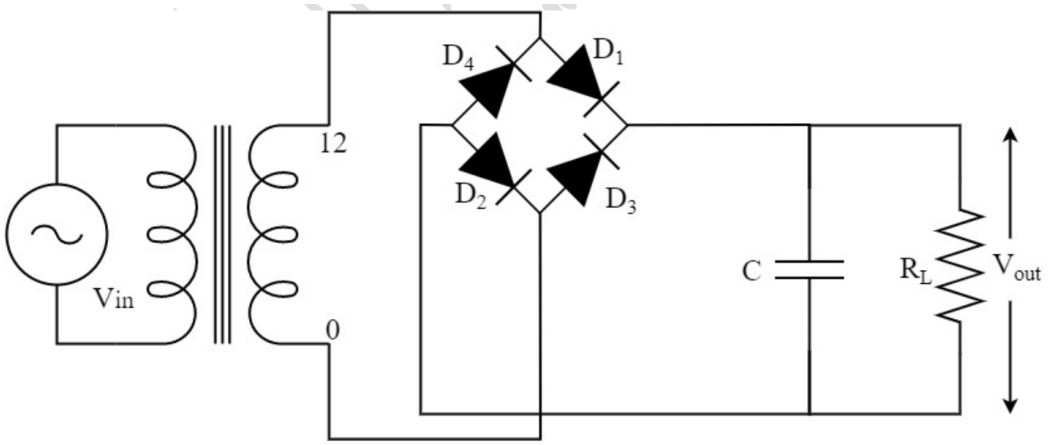


Figure (20): Full-wave rectifier with capacitor

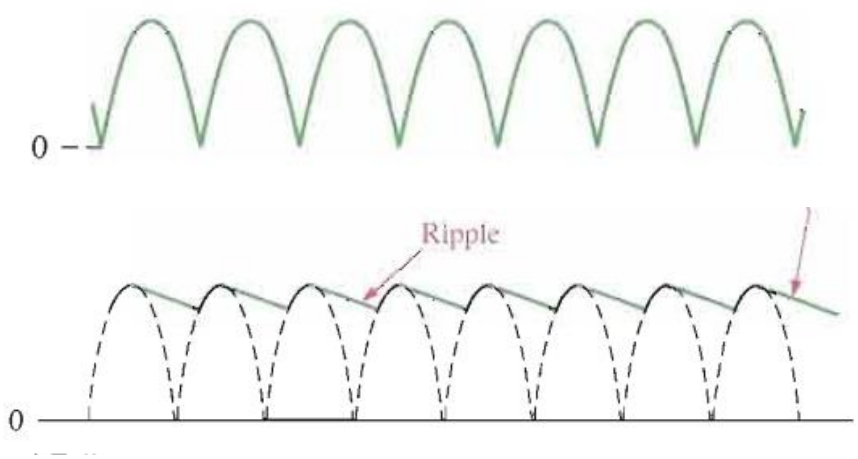


Figure (21): Full-wave ripple voltage waveform

Ripple Factor

The ripple factor (r) is an indication of the effectiveness of the filter and is defined as

$$r = \frac{V_{r(pp)}}{V_{DC}}$$

Where the peak-to-peak ripple voltage and V_{DC} is the DC (average) value of the filter's output voltage, as illustrated in Figure (22). The lower the ripple factor, the better the filter. The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load resistance.

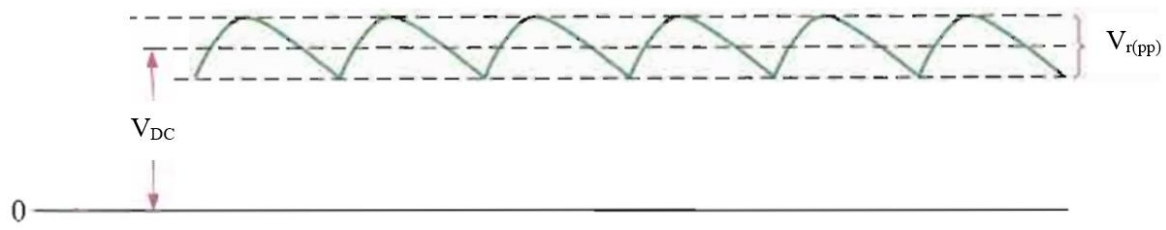


Figure (22): The calculation of the ripple factor

Clipper circuit

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

Figure (23) shows the output is defined across the series combination of the power supply and the diode, not across the resistor R.

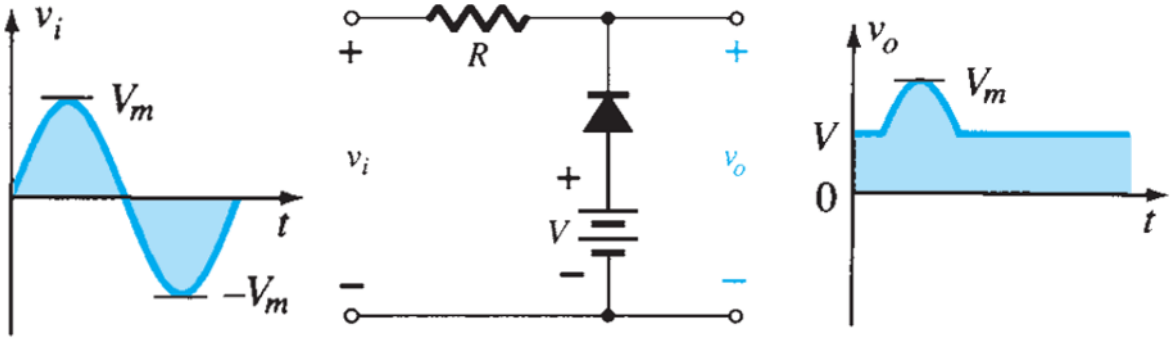


Figure (23): Clipper operation

The polarity of the DC supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the V_{DC} supply, requiring that the output be fixed at V_{DC}. In other words, when the diode is on the output will be V_{DC}. Other than that, when the diode is an open circuit, the current through the series network will be 0mA and the voltage drop across the resistor will be 0V. That will result in

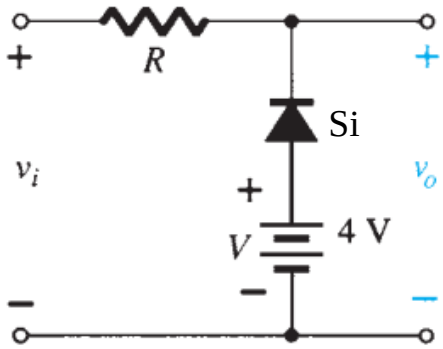
Vo* = *Vi whenever the diode is off.

The transition level of the input voltage can be found from Figure (23) by substituting the short-circuit equivalent and remembering the diode current is 0mA at the instant of transition. The result is a change in state when

$$\boldsymbol{Vi = V_{DC}}$$

In Figure (23) the transition level is drawn along with Vo = V_{DC} when the diode is on. For Vi ≥ V_{DC}, Vo = V_{DC}, and the waveform is simply repeated on the output plot.

Example: Determine and plot the output of this circuit



Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$-V_O + V_{DC} - V_k = 0$$

$$V_O = V_{DC} - V_k$$

$$V_O = 4 - 0.7 = 3.3V$$

The resulting output waveform appears in the next figure. Note that the only effect of V_k was to drop the transition level to 3.3 from 4V.

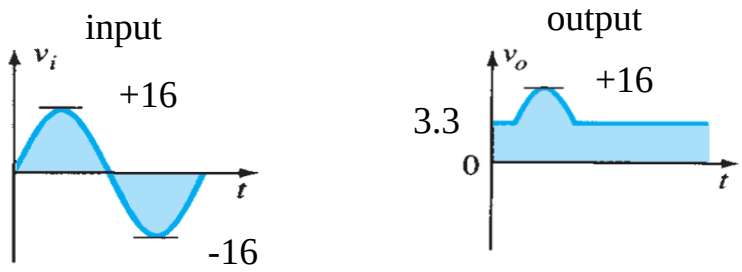


Figure (24) shows another shape forming in the clipper circuit that the diode will be in the "on" state for a portion of the positive region of the input signal. When the diode is in its short-circuit state the output voltage will be directly across the

V_{DC} supply, requiring that the output be fixed at V_{DC}. Other than that, when the diode is an open circuit, the current through the series network will be 0mA and the voltage drop across the resistor will be 0V. That will result in

Vo* = *Vi whenever the diode is off.

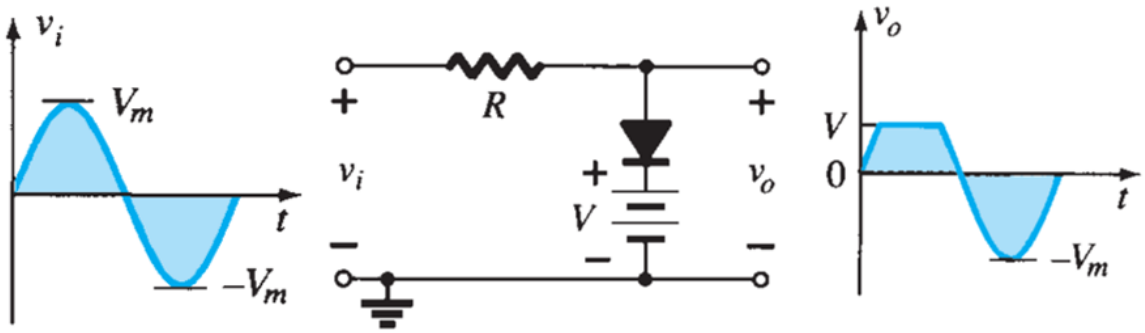
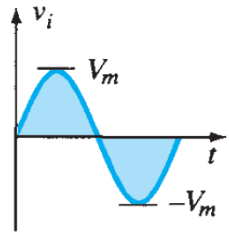


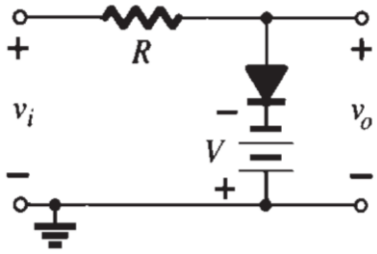
Figure (24): Clipper operation

Solve: Sketch the output waveforms for the next circuits:

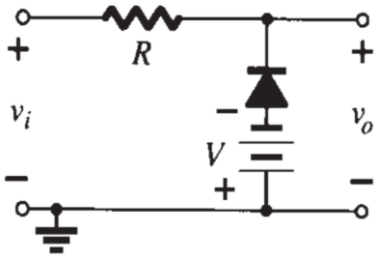
Input waveform



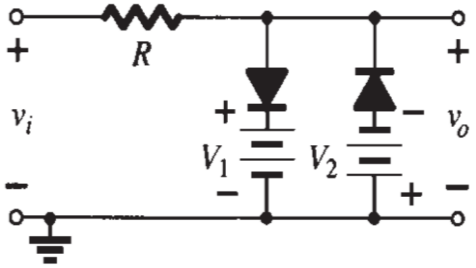
A



B



C



Clamper circuit

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different DC level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a DC supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $t = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is provided in Figure (25). It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal.

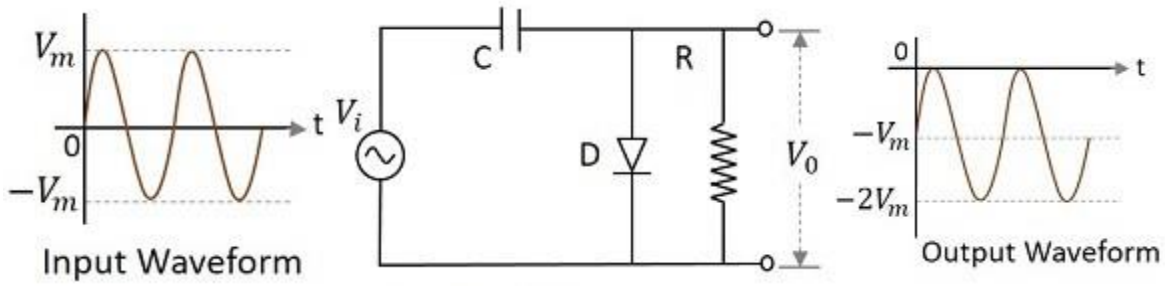


Figure (25): Negative Clamper circuit operation

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Figure 25 the diode will be forward biased for the positive portion of the applied signal. For the positive wave the network will appear as shown in Figure 25.

The short-circuit equivalent for the diode will result in *Vo* < 0V for this time interval, as shown in the sketch of *Vo* in Figure 25. During this same interval of time, the time constant determined by t = *RC* is very small because the resistor *R* has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of *V* volts as shown in Fig. 25 with the polarity indicated.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for Vo to ensure that the proper levels are obtained.

When the input switches to the V state, the network will appear with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period.

Since Vo is in parallel with the diode and resistor, it can also be drawn in the alternative position. Applying Kirchhoff's voltage law around the input loop results in

$$-V_i - V - V_o = 0 \qquad where\ V_i = V$$

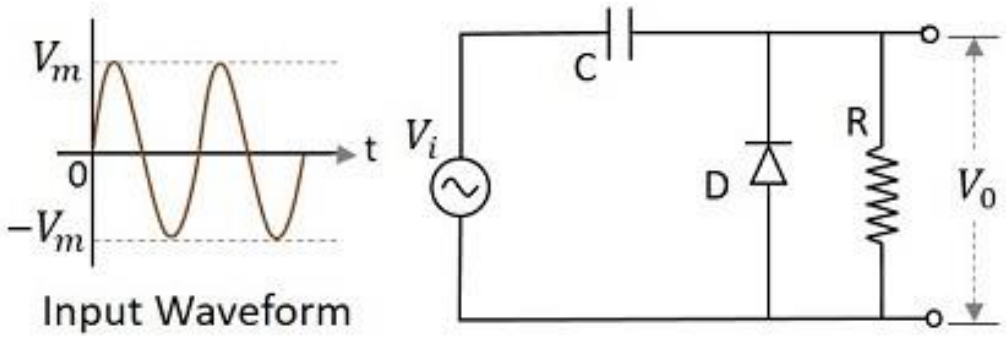
$$V_O = -2V$$

The negative sign results from the fact that the polarity of 2V is opposite to the polarity defined for Vo. The resulting output waveform appears in Figure 25 with the input signal.

The output signal is clamped to 0 V for the positive wave but maintains the same total swing (2V) as the input.

Step 5: Check that the total swing of the output matches that of the input. This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

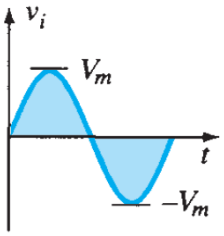
Solve: Sketch the output waveform for the next circuit:



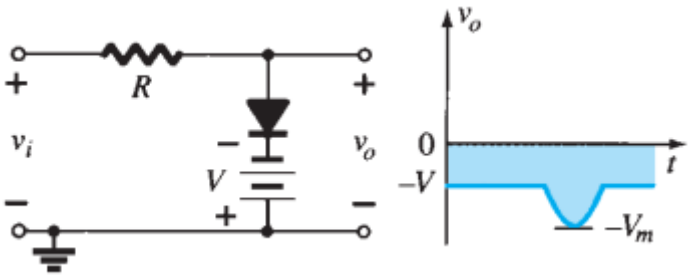
Homework Solution

Solve: Sketch the output waveforms for the next circuits:

Input waveform



A



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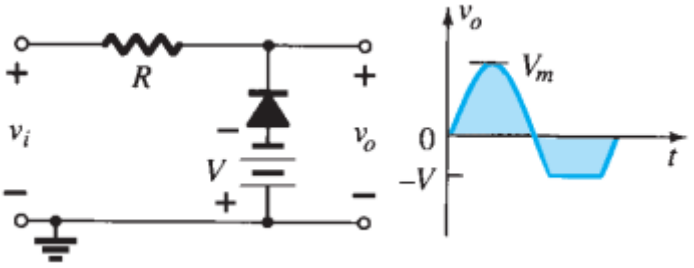

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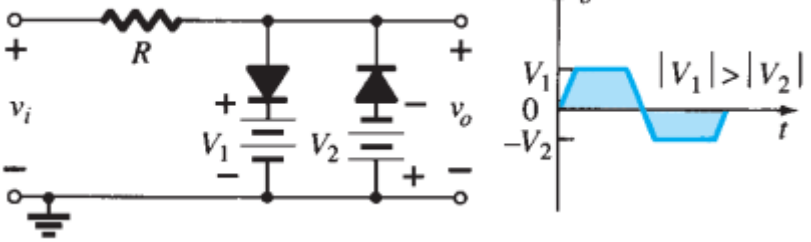

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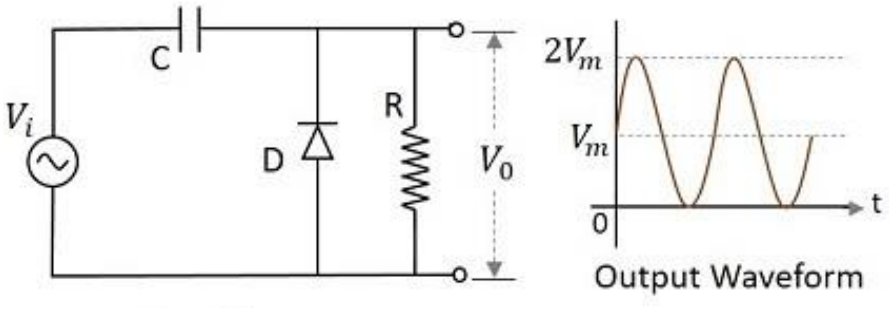


Transistor

Transistor Construction

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, and the latter is called a pnp transistor. Both are shown in Figure (1) with the proper dc biasing. The three regions are called *emitter*, *base*, and *collector*. The DC biasing is necessary to establish the proper region of operation. The base region is lightly doped and very thin compared to the heavily doped emitter and the moderately doped collector regions.

For the biasing shown in Figure (1) the terminals have been indicated by the capital letters E for emitter, C for collector, and B for base. The pn junction joining the base region and the emitter region is called the base-emitter junction. The pn junction joining the base region and the collector region is called the base-collector Junction. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor.

The abbreviation BJT, from bipolar junction transistor, is often applied to this three-terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device.

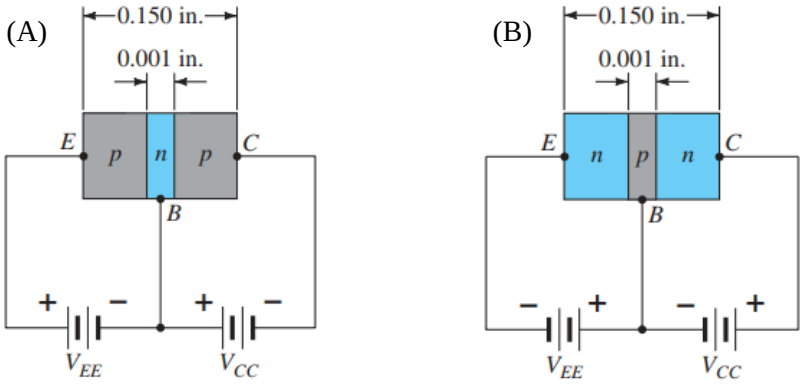


Figure (1): Types of transistors: (A) pnp; (B) npn

Transistor Operation

The basic operation of the transistor will now be described using the *pnp* transistor of Figure (1-A). The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Figure (2-a) the *pnp* transistor has been redrawn without the base-to collector bias. Note the similarities between this situation and that of the *forward-biased* diode. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

Let us now remove the base-to-emitter bias of the *pnp* transistor of Fig. (2-a) as shown in Fig. (2-b). Consider the similarities between this situation and that of the *reverse-biased* diode. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. (2-b). In summary, therefore:

One p–n junction of a transistor is reverse-biased, whereas the other is forward-biased.

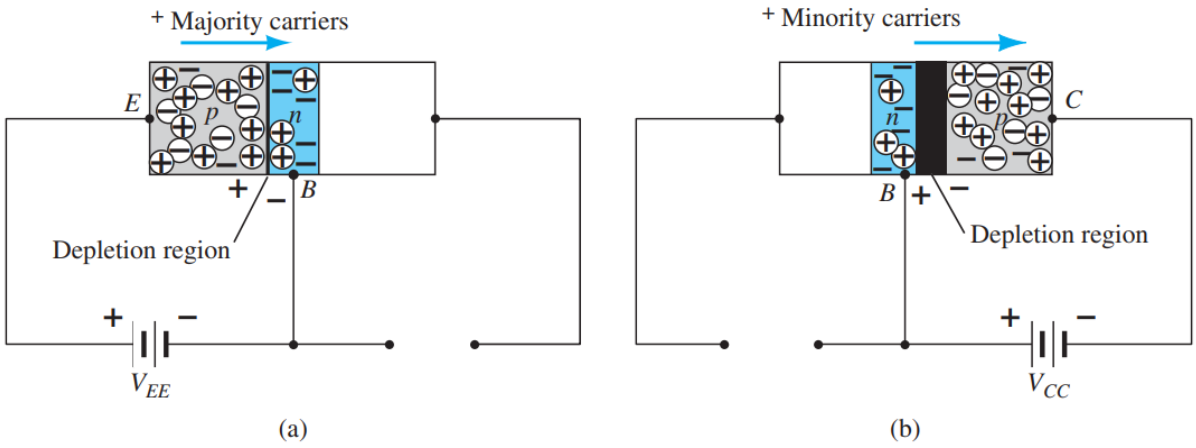


Figure (2): Biasing a transistor: (a) forward-bias; (b) reverse-bias

In Figure (3) both biasing potentials have been applied to a pnp transistor, with the resulting majority- and minority-carrier flows indicated. Note in Fig. (3) the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. (3), a large number of majority carriers will diffuse across the forward-biased p–n junction into the n-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the p-type material. Since the sandwiched n-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal.

The magnitude of the base current is typically on the order of microamperes, as compared to milli-amperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Figure (3). The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. (3).

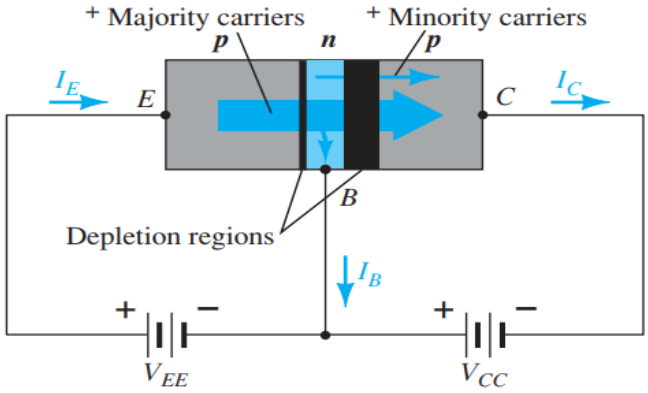


Figure (3): Majority and minority carrier flow of a pnp transistor

Applying Kirchhoff's current law to the transistor of Fig. (3) as if it were a single node, we obtain

$$I_E = I_C + I_B$$

and find that the emitter current is the sum of the collector and base currents as indicated in Fig. (4).

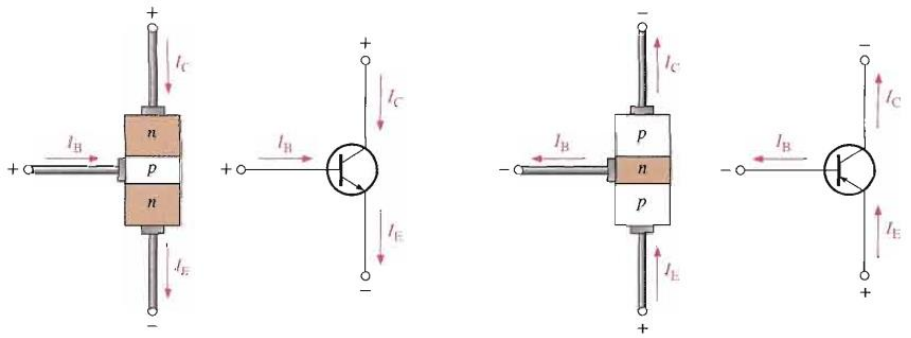


Figure (4): Transistor current flow

Transistor Parameters

Two important parameters, β_{DC} (DC current gain) and α are introduced and used to analyze a transistor circuit. Also, transistor characteristic curves are covered, and you will learn how a transistor's operation can be determined from these curves.

Figure (5) shows both npn and pnp circuits with the connection of resistances and power supplies.

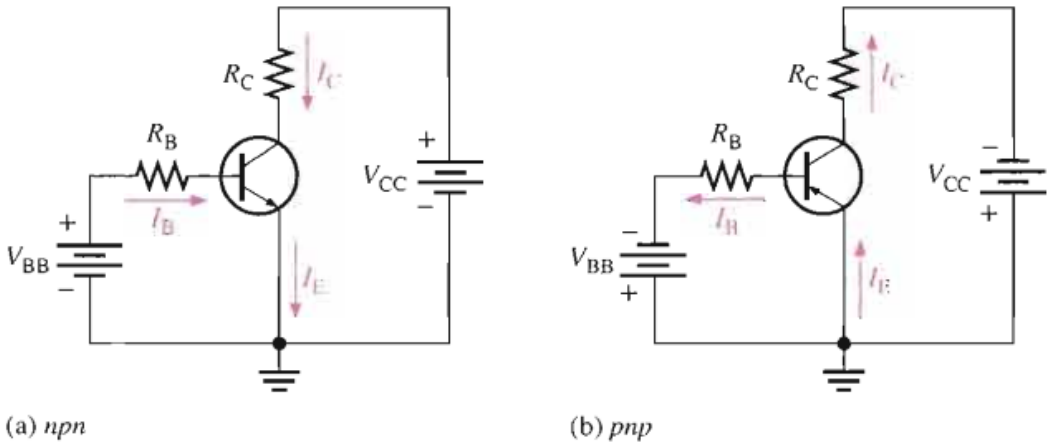


Figure (5) a) npn; and b) pnp circuits

DC Beta

The ratio of the DC collector current (I_C) to the DC base current (I_B) is the DC beta (β_{DC}), which is the dc current gain of a transistor.

$$\beta_{DC} = \frac{I_C}{I_B}$$

DC Alpha

The ratio of the DC collector current (I_C) to the DC emitter current (I_E) is the DC alpha (α). The alpha is a less-used parameter than beta in transistor circuits.

$$\alpha = \frac{I_C}{I_E}$$

Example: Determine β_{DC} and α for a transistor where $I_B = 50\mu A$ and $I_C = 3.65mA$.

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.65 \times 10^{-3}}{50 \times 10^{-6}} = 73$$

$$I_E = I_C + I_B = 3.65 + 50 \times 10^{-3}$$

$$I_E = 3.7mA$$

$$\alpha = \frac{I_C}{I_E} = \frac{3.65 \times 10^{-3}}{3.7 \times 10^{-3}} = 0.98$$

Current and Voltage Analysis

Consider the basic transistor bias circuit configuration in Figure (6). Three transistor DC currents and three DC voltages can be identified.

- I_B: DC base current
- I_E: DC emitter current
- I_C: DC collector current
- V_{BE}: DC voltage at base with respect to emitter
- V_{CB}: DC voltage at collector with respect to base
- V_{CE}: DC voltage at collector with respect to emitter

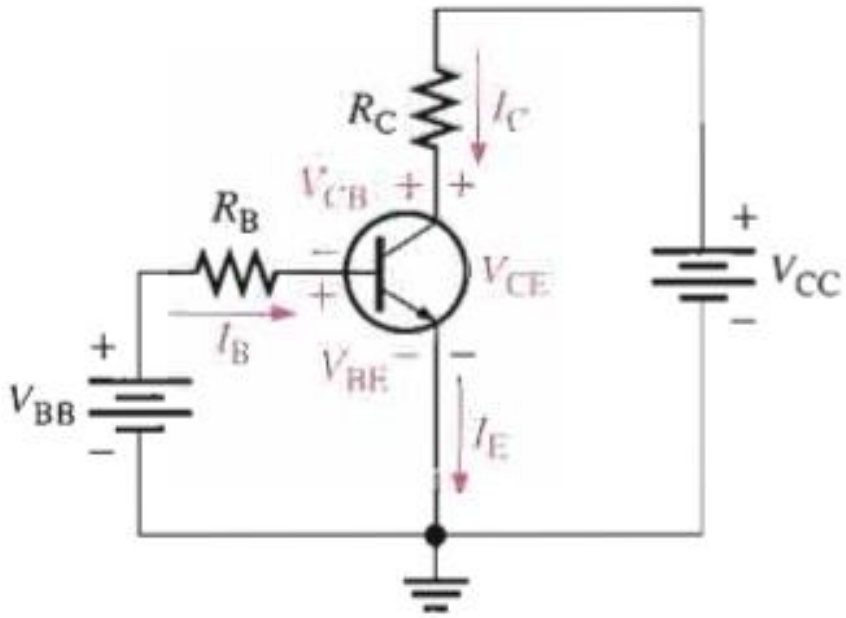


Figure (6): Transistor currents and voltages

V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of

$$V_{BE} \cong 0.7V$$

Although in an actual transistor V_{BE} can be higher than 0.7V and is dependent on current, we will use 0.7V throughout this text in order to simplify the analysis of the basic concepts. Since the emitter is at ground (0V), by Kirchhoff's voltage law, the voltage across R_B is

$$V_B = V_{BB} - V_{BE}$$

Also, by ohm's law,

$$V_B = I_B R_B$$

Substituting for V_B yields

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for I_B,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_C$$

Since the drop across R_C is

$$V_C = I_C R_C$$

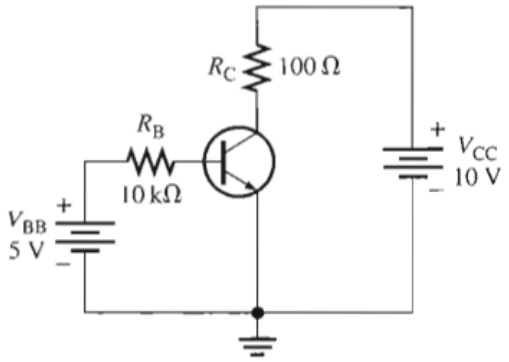
The voltage at the collector can be written as

$$V_{CE} = V_{CC} - I_C R_C$$

The voltage across the reverse-biased collector-base junction is

$$V_{CB} = V_{CE} - V_{BE}$$

Example: Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit of the next Figure. The transistor has a $\beta_{DC} = 150$.



Solution:

Consider $V_{BE} = 0.7V$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 - 0.7}{10 \times 10^3} = 0.43mA = 430\mu A$$

$$I_C = \beta_{DC} I_B = 150 \times 0.43 \times 10^{-3} = 64.5mA$$

$$I_E = I_C + I_B = 64.5mA + 0.43mA = 64.93mA$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - (64.5 \times 10^{-3} \times 100) = 10 - 6.45 = 3.55V$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = 2.85V$$

Homework: Determine I_B, I_C, I_E, V_{CE}, and V_{CB} for the following values: R_B=22kΩ, Rc=220Ω, V_{BB}=6V, V_{CC}=9V, and $\beta_{DC} = 90$.

Collector Characteristic Curves

Using a circuit like that shown in Figure (7), you can generate a set of collector characteristic curves that show how the collector current, I_C, varies with the collector-to-emitter voltage, V_{CE}, for specified values of base current, I_B. Notice in the circuit diagram that both V_{BB} and V_{CC} are variable sources of voltage.

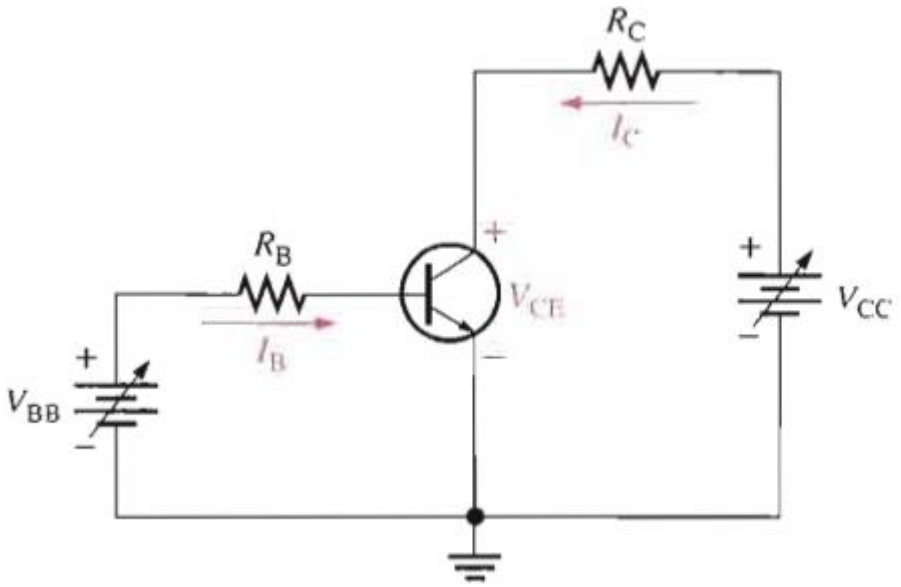


Figure (7): Transistor circuit

Assume that V_{BB} is set to produce a certain value of I_B and when V_{CC} is increased, V_{CE} increases gradually as the collector current increases as shown in Figure (8).

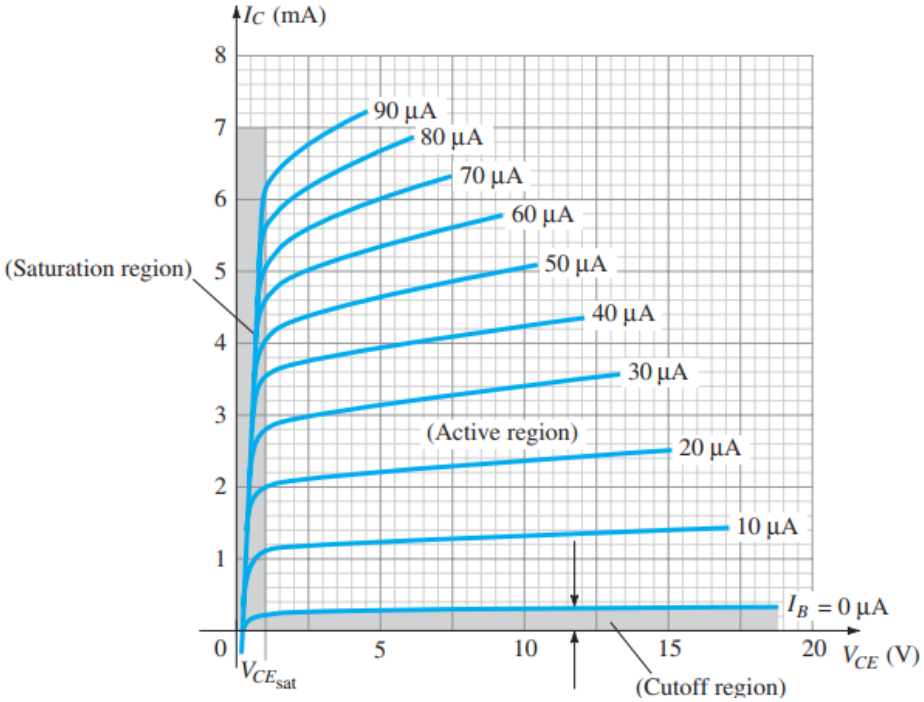


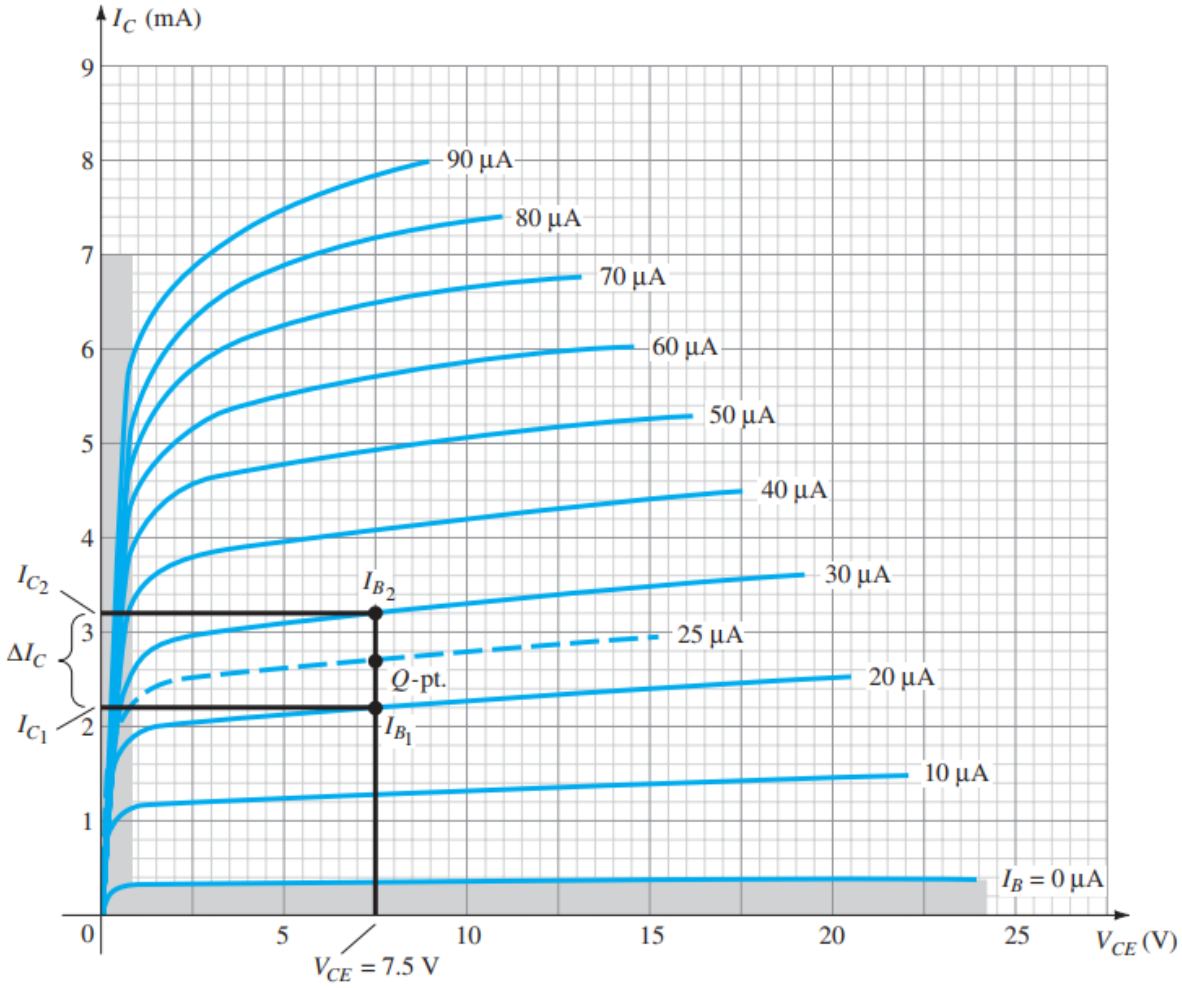
Figure (8): Collector Characteristic curve

From the curves of Fig. (8), if V_{CE} is constant value, we can calculate the AC gain by:

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}constant}$$

Example: Determine β_{AC} and β_{DC} for Fig. (8) when $V_{CE} = 7.5V$.

Solution:



$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}constant} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

$$\beta_{AC} = \frac{3.2 \times 10^{-3} - 2.2 \times 10^{-3}}{30 \times 10^{-6} - 20 \times 10^{-6}} = \frac{(3.2 - 2.2) \times 10^{-3}}{(30 - 20) \times 10^{-6}}$$

$$\beta_{AC} = 100$$

If we determine the DC beta at the Q-point, we obtain

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{2.7 \times 10^{-3}}{25 \times 10^{-6}} = 108$$

Junction Field Effect Transistor (JFET)

The JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor there was two types of transistor: npn *and pnp* transistors. For the JFET the *n*-channel and *p*-channel devices will be the prominent devices.

JFET Construction

The basic construction of the *n*-channel JFET is shown in Figure (9). Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. (9), that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

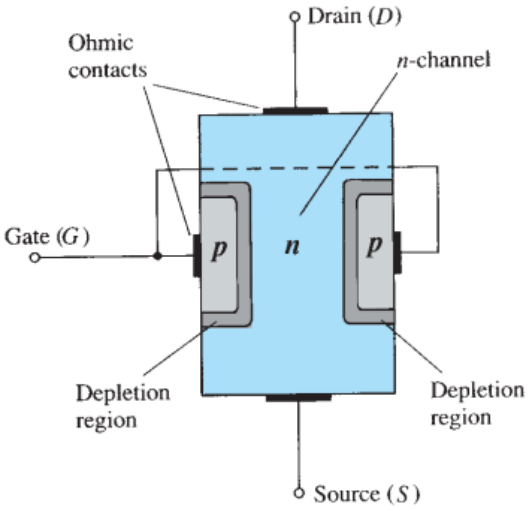


Figure (9): Junction field-effect transistor (JFET).

JFET Operation

To illustrate the operation of a JFET, Figure (10) shows DC bias voltages applied to an N-channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source.

The JFET is always operated with the gate-source pn junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the N-channel and thus increases its resistance by restricting the channel width.

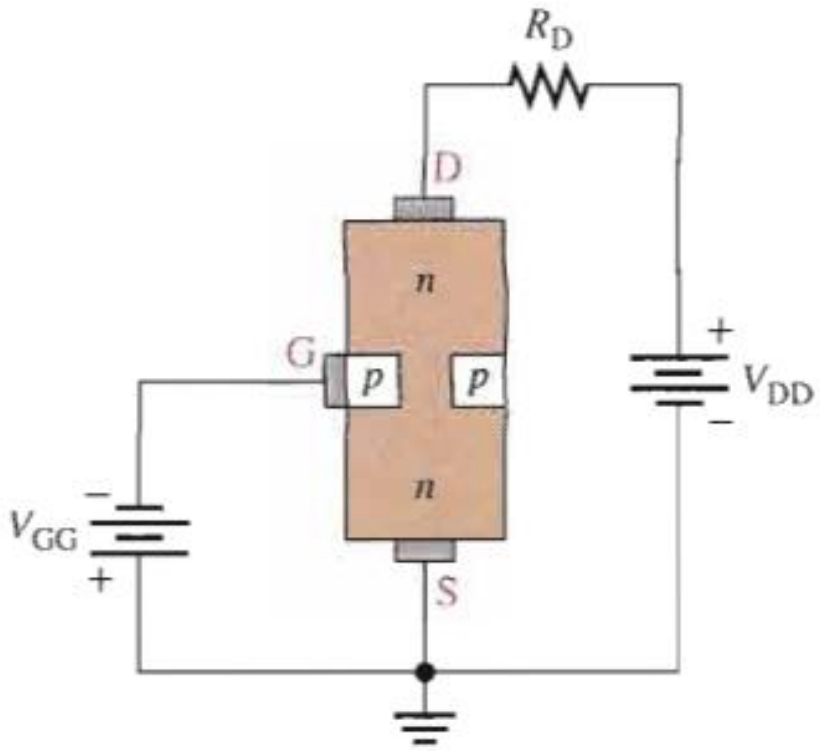
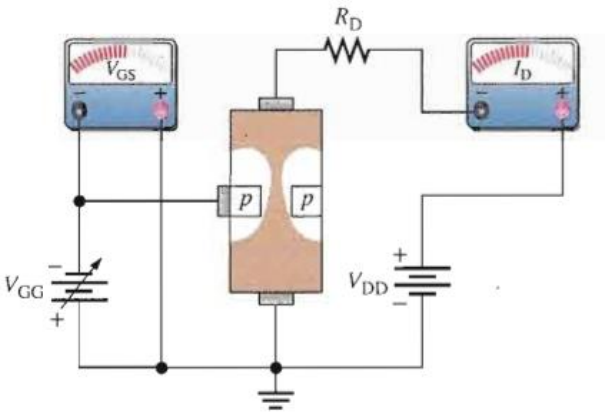
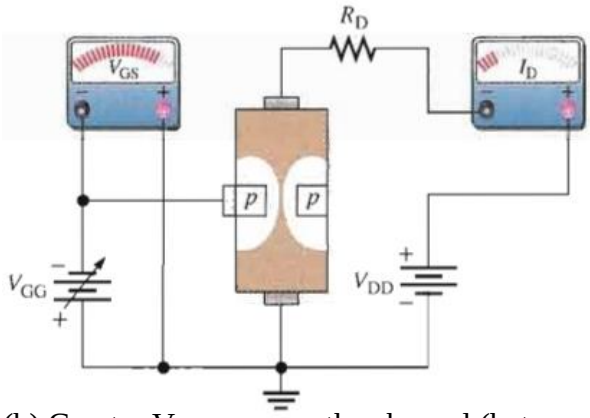


Figure (10): Biased N-channel JFET

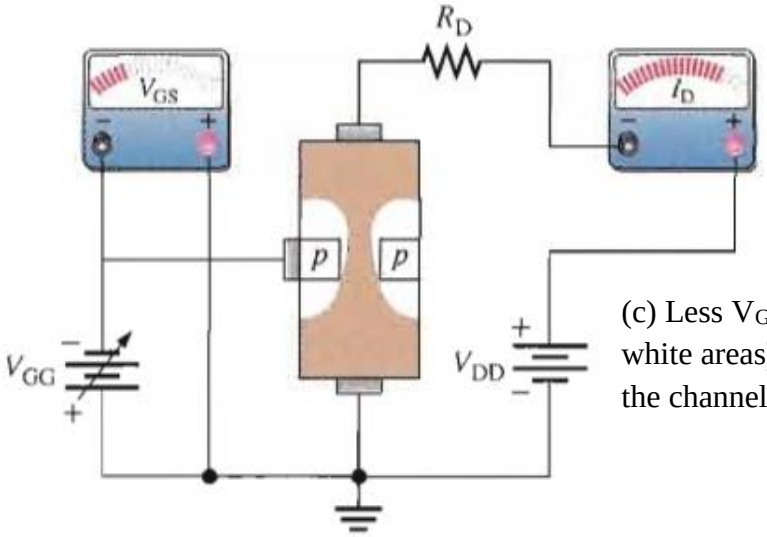
The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D. Figure (11) illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.



(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D



(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D

Figure (11): Effects of V_{GS} on channel width, resistance, and drain current when $V_{GG} = V_{GS}$

JFET Symbols

The schematic symbols for both N-channel and P-channel JFETs are shown in Figure (12). Notice that the arrow on the gate points "in" for n-channel and "out" for p-channel.

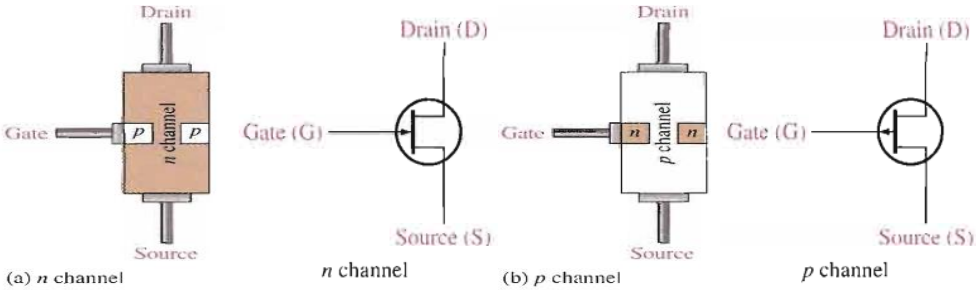
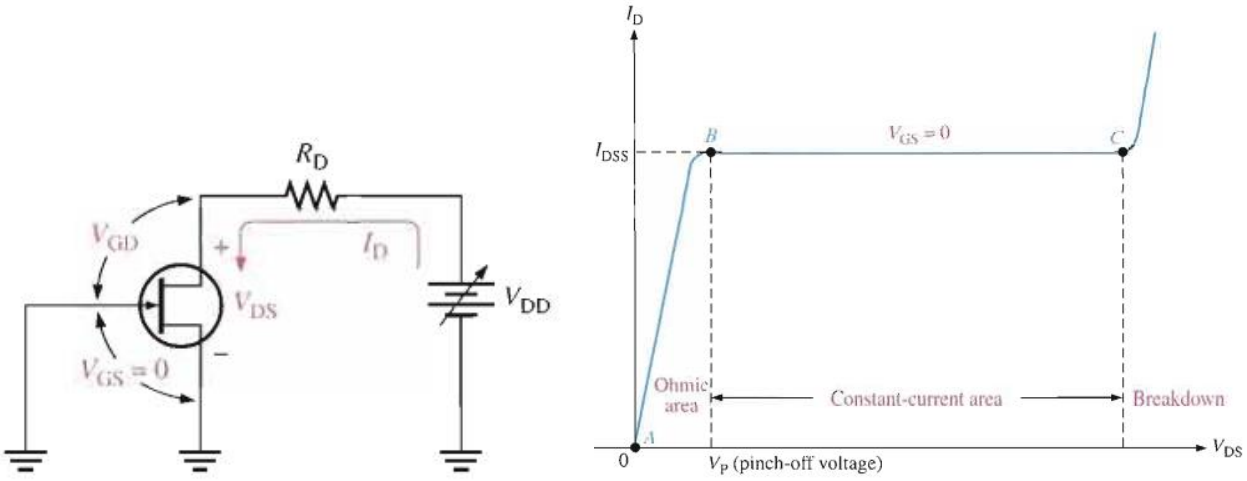


Figure (12): JFET schematic symbols

JFET Characteristic

Consider the case when the gate-to-source voltage is zero (V_{GS} = 0V). This is produced by shorting the gate to the source, as in Figure (13-a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0V, I_D will increase proportionally, as shown in the graph of Figure (13-b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic area because V_{DS} and I_D are related by Ohm's law.



(a) JFET with V_{GS} = 0V and variable V_{DS} (V_{DD}) (b) Drain Characteristic

Figure (13): The drain characteristic curve if JFET for V_{GS} = 0V

At point B in Figure (13-b), the curve levels off and I_D becomes essentially constant. As V_{DS} increases from point B to point C, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

Pinch-Off Voltage

For V_{GS} = 0V, the value of V_{DS} at which I_D becomes essentially constant (point B on the curve in Figure (13-b)) is the pinch-off voltage, V_p. For a given JFET, V_p has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (Drain to Source current with gate Shorted) and is always specified on JFET data sheets. I_{DSS} is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, V_{GS} = 0V.

As shown in the graph in Figure (13-b), ***breakdown*** occurs at point C when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the constant-current area (between points B and C on the graph).

V_{GS} Controls I_D

Let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure (14-a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure (14-b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P.

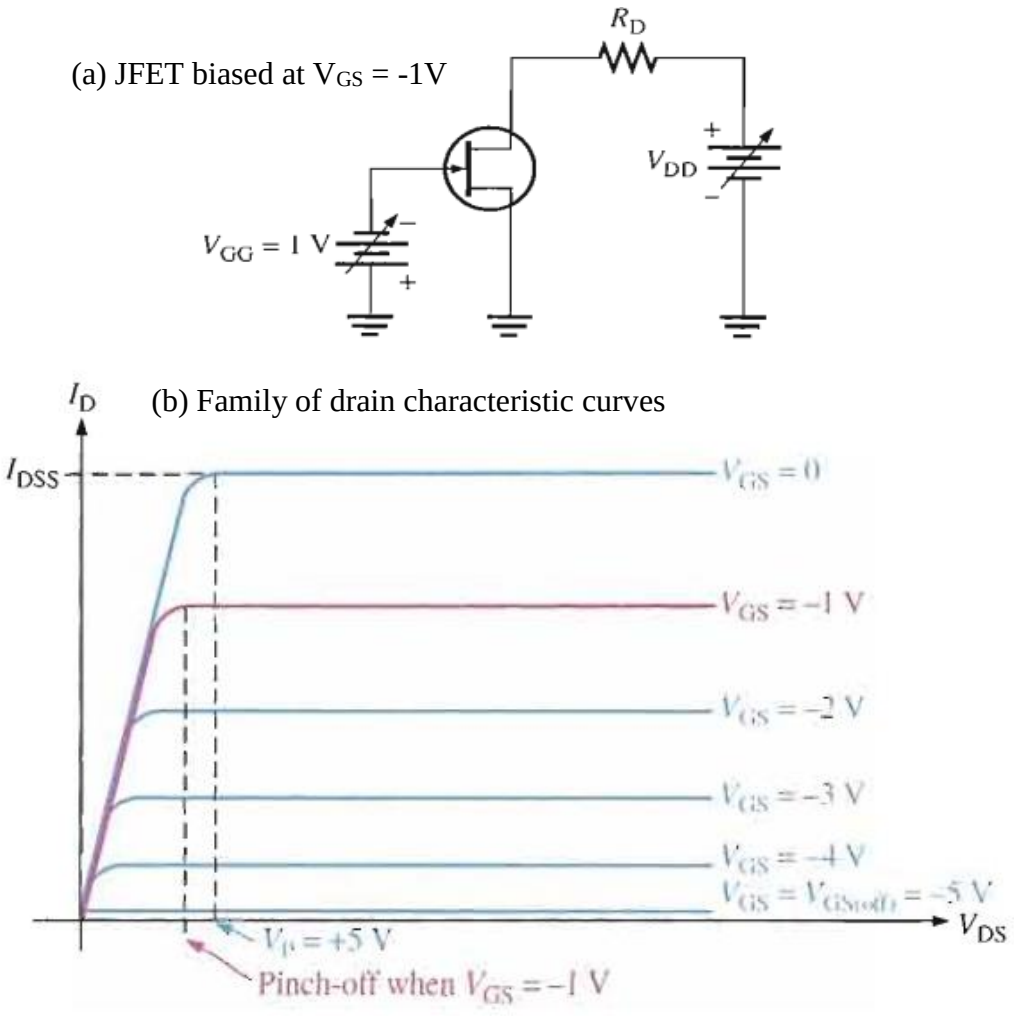


Figure (14): Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET differs from the JFET in that it has no PN junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are depletion (D) and enhancement (E). The terms depletion and enhancement define their basic mode of operation.

Depletion MOSFET (D-MOSFET)

One type of MOSFET is the depletion MOSFET (D-MOSFET), and Figure (15) illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both n-channel and p-channel devices are shown in Fig. (15). We will use the n-channel device to describe the basic operation.

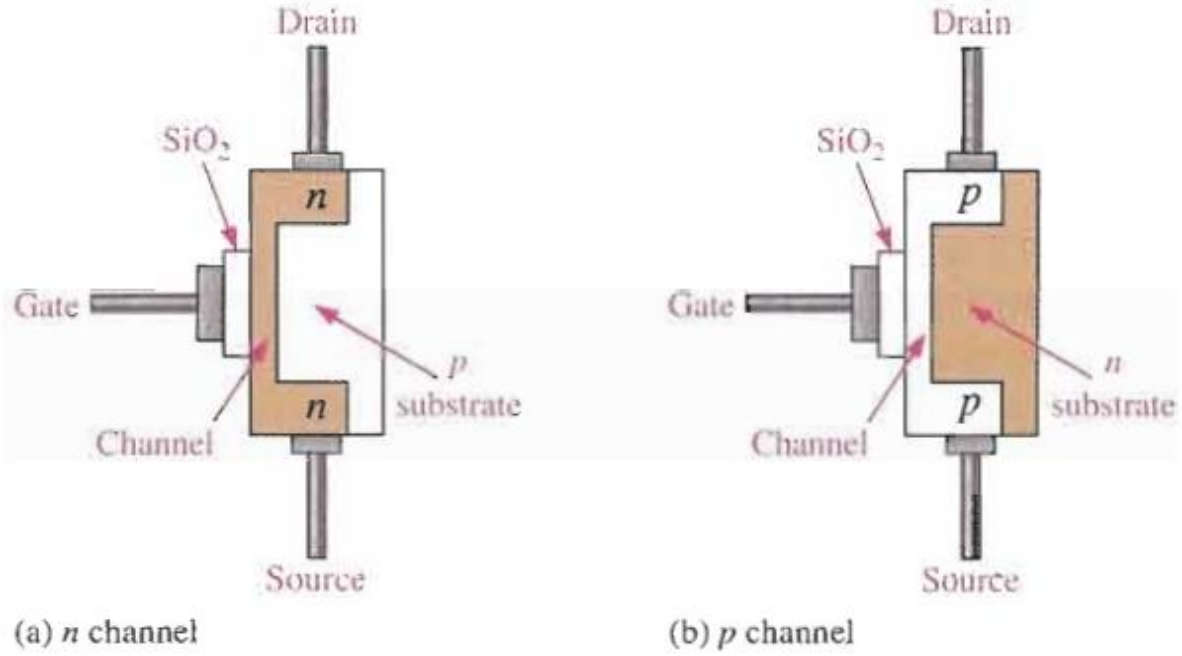


Figure (15): Basic structure of D-MOSFETs

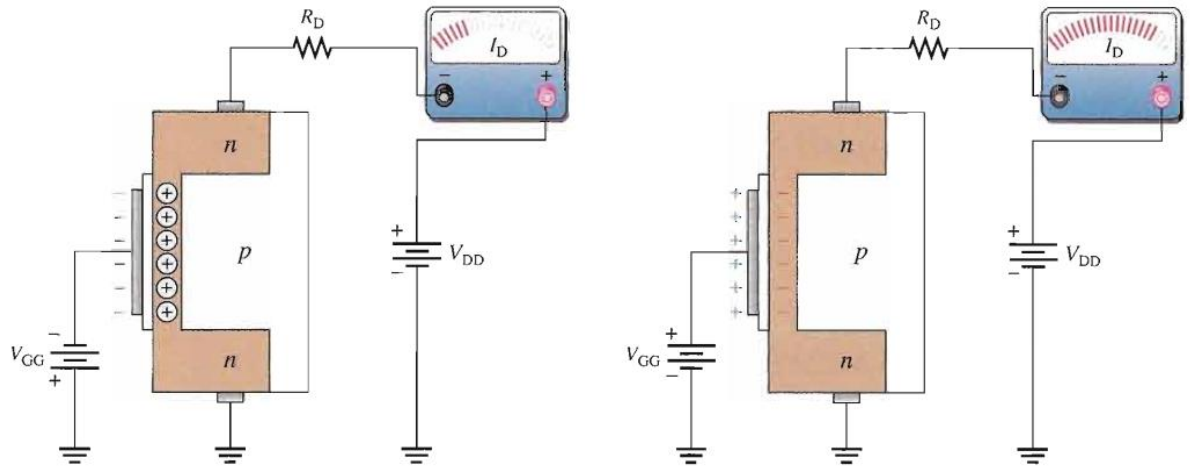
The D-MOSFET can be operated in either of two modes, the depletion mode or the enhancement mode and is sometimes called a depletion/enhancement MOSFET. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The n-channel MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied.

Depletion Mode

Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure (16-a). Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of above zero.

Enhancement Mode

With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure (16-b).



(a) Depletion mode: V_{GS} negative and less than $V_{GS(off)}$ (b) Enhancement mode: V_{GS} positive

Figure (16): Operation of n-channel D-MOSFET

D-MOSFET Symbols

The schematic symbols for both the n-channel and the p-channel depletion MOSFETs are shown in Figure (17). The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin. An inward-pointing substrate arrow is for n-channel, and an out ward-pointing arrow is for p-channel.

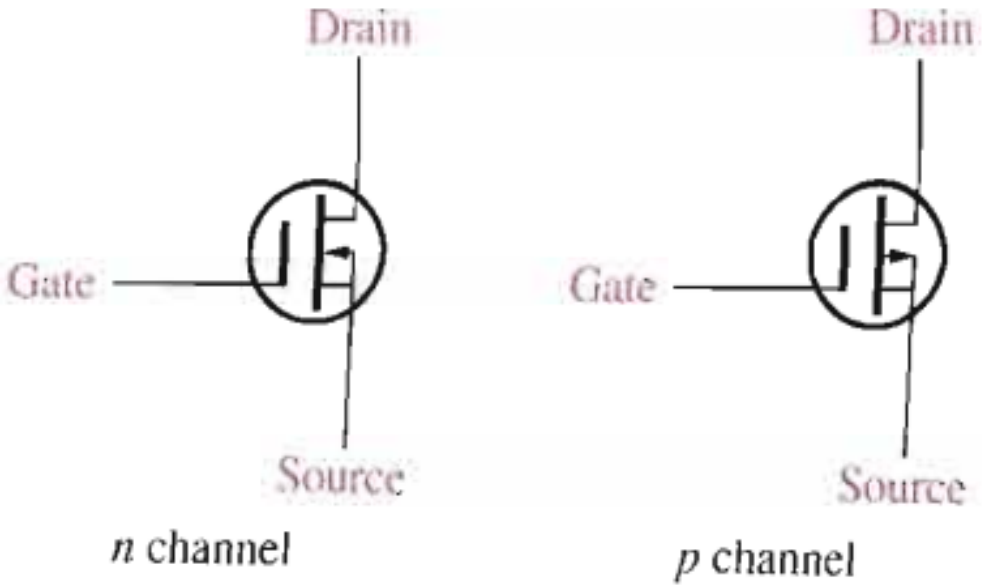
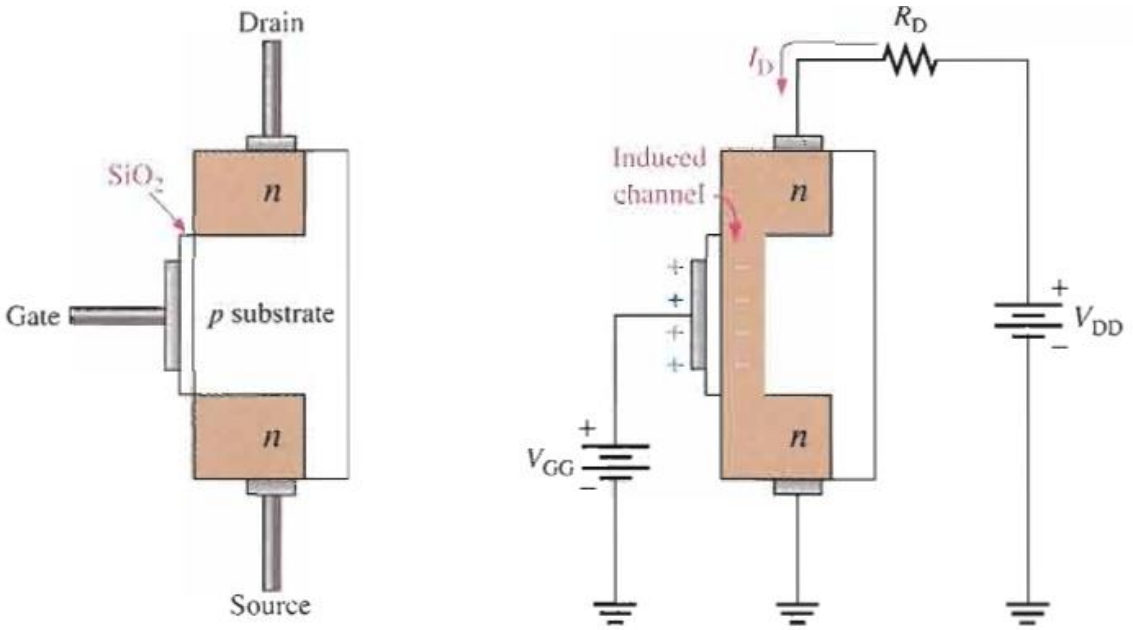


Figure (17): D-MOSFET schematic symbols

Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET in that it has no structural channel. Notice in Figure (18-a) that the substrate extends completely to the SiO_2 layer. For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure (18-b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.



(a) Basic construction

(b) Induced channel ($V_{GS} > V_{GS(th)}$)

Figure (18): The basic E-MOSFET construction and operation (n-channel)

E-MOSFET Symbol

The schematic symbols for the n-channel and p-channel E-MOSFETs are shown in Figure (19). The broken lines symbolize the absence of a physical channel. Like the D-MOSFET, some devices have a separate substrate connection.

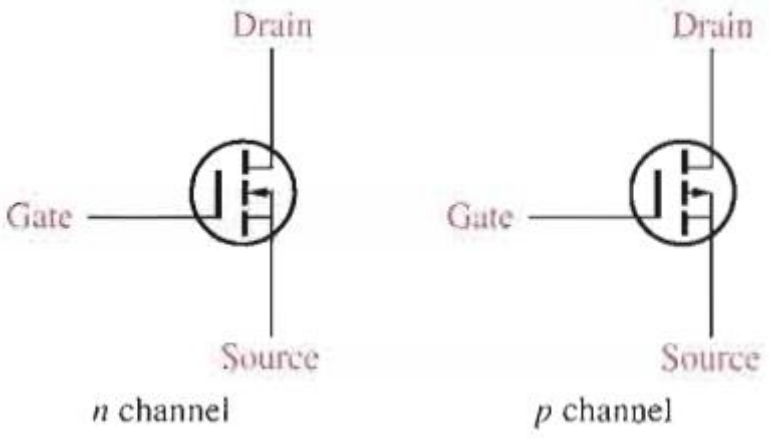


Figure (19): E-MOSFET schematic symbols